In Clear Electronics

WWW.IC-1000.COM

# THE DATASHEET OF FPGA


www.ic-1000.com info@ic-1000.com

+00852-56412601 +00852-56412601

Unit B，13/F，Shing Lee Commercial Building
No.8 Wing Kut Street，Central HK

# Stratix V Device Datasheet

SV53001-4.1

This document covers the electrical and switching characteristics for Stratix® V devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

For information regarding the densities and packages of devices in the Stratix V family, refer to the *Stratix V Device Overview*.

## Electrical Characteristics

The following sections describe the electrical characteristics of Stratix V devices.

### Operating Conditions

When you use Stratix V devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix V devices, you must consider the operating requirements described in this chapter.

Stratix V devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –1 (fastest), –2, –3, and –4 core speed grades. Industrial devices are offered in –2, –3, and –4 core speed grades. Stratix V E devices are offered based on core speed grades while Stratix V GX, GS, and GT devices are also offered in -1, -2, and -3 transceiver speed grades.

Table 1 lists the industrial and commercial speed grades for the Stratix V GX and Stratix V GS devices.

**Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering** *(1), (2), (3)* **(Part 1 of 2)**

| Transceiver Speed Grade | Core Speed Grade | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L | I3YY | I4 |
| 1<br>GX channel—14.1 Gbps | Yes | Yes | — | — | Yes | — | — | — |
| 2<br>GX channel—12.5 Gbps | Yes | Yes | Yes | — | Yes | Yes | — | — |

101 Innovation Drive
San Jose, CA 95134
www.altera.com

**Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering (1), (2), (3) (Part 2 of 2)**

| Transceiver Speed Grade | Core Speed Grade | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L | I3YY | I4 |
| 3<br>GX channel—8.5 Gbps | — | Yes | Yes | Yes | — | Yes | Yes (4) | Yes |

**Notes to Table 1:**

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices.

**Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering (1), (2)**

| Transceiver Speed Grade | Core Speed Grade | | | |
|---|---|---|---|---|
| | C1 | C2 | I2 | I3 |
| 2<br>GX channel—12.5 Gbps<br>GT channel—28.05 Gbps | Yes | Yes | — | — |
| 3<br>GX channel—12.5 Gbps<br>GT channel—25.78 Gbps | Yes | Yes | Yes | Yes |

**Notes to Table 2:**

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

## Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

CAUTION

Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 1 of 2)**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Power supply for core voltage and periphery circuitry | –0.5 | 1.35 | V |
| $V_{CCPT}$ | Power supply for programmable power technology | –0.5 | 1.8 | V |
| $V_{CCPGM}$ | Power supply for configuration pins | –0.5 | 3.9 | V |
| $V_{CC\_AUX}$ | Auxiliary supply for the programmable power technology | –0.5 | 3.4 | V |
| $V_{CCBAT}$ | Battery back-up power supply for design security volatile key register | –0.5 | 3.9 | V |
| $V_{CCPD}$ | I/O pre-driver power supply | –0.5 | 3.9 | V |
| $V_{CCIO}$ | I/O power supply | –0.5 | 3.9 | V |

**Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCD\_FPLL}$ | PLL digital power supply | –0.5 | 1.8 | V |
| $V_{CCA\_FPLL}$ | PLL analog power supply | –0.5 | 3.4 | V |
| $V_I$ | DC input voltage | –0.5 | 3.8 | V |
| $T_J$ | Operating junction temperature | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (No bias) | –65 | 150 | °C |
| $I_{OUT}$ | DC output current per pin | –25 | 40 | mA |

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

**Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices**

| Symbol | Description | Devices | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ | Transceiver channel PLL power supply (left side) | GX, GS, GT | –0.5 | 3.75 | V |
| $V_{CCA\_GXBR}$ | Transceiver channel PLL power supply (right side) | GX, GS | –0.5 | 3.75 | V |
| $V_{CCA\_GTBR}$ | Transceiver channel PLL power supply (right side) | GT | –0.5 | 3.75 | V |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHIP\_R}$ | Transceiver hard IP power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GXBL}$ | Receiver analog power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GXBR}$ | Receiver analog power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GTBR}$ | Receiver analog power supply for GT channels (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCT\_GXBL}$ | Transmitter analog power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCT\_GXBR}$ | Transmitter analog power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCT\_GTBR}$ | Transmitter analog power supply for GT channels (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCL\_GTBR}$ | Transmitter clock network power supply (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power supply (left side) | GX, GS, GT | –0.5 | 1.8 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power supply (right side) | GX, GS, GT | –0.5 | 1.8 | V |

### Maximum Allowed Overshoot and Undershoot Voltage

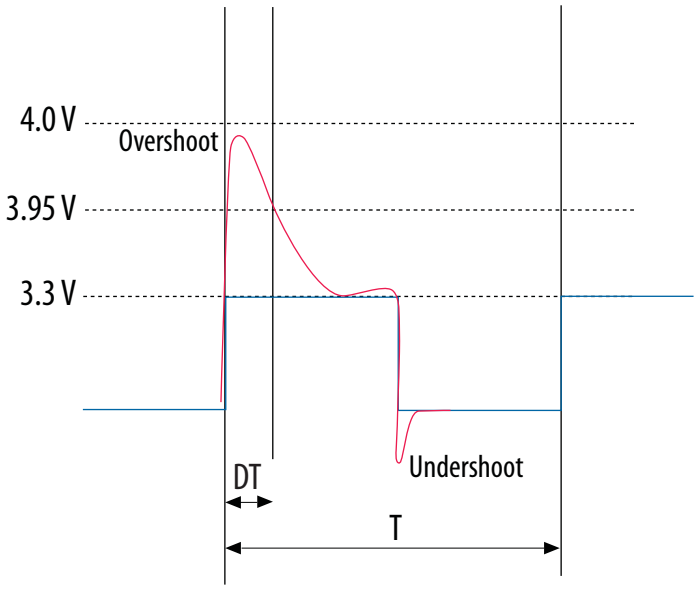
During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

| Symbol | Description | Condition (V) | Overshoot Duration as % @ $T_J$ = 100°C | Unit |
|---|---|---|---|---|
| Vi (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 64 | % |
| | | 3.9 | 36 | % |
| | | 3.95 | 21 | % |
| | | 4 | 12 | % |
| | | 4.05 | 7 | % |
| | | 4.1 | 4 | % |
| | | 4.15 | 2 | % |
| | | 4.2 | 1 | % |

**Figure 1. Stratix V Device Overshoot Duration**



## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

| Symbol | Description | Condition | Min (4) | Typ | Max (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades) | — | 0.87 | 0.9 | 0.93 | V |
| | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) (3) | — | 0.82 | 0.85 | 0.88 | V |
| $V_{CCPT}$ | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| $V_{CC\_AUX}$ | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPD}$ (1) | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCPGM}$ | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA\_FPLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_FPLL}$ | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| $V_{CCBAT}$ (2) | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Condition | Min (4) | Typ | Max (4) | Unit |
|---|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

**Notes to Table 6:**

(1) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect $V_{CCBAT}$ to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors $V_{CCBAT}$. Stratix V devices will not exit POR if $V_{CCBAT}$ stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

| Symbol | Description | Devices | Minimum (4) | Typical | Maximum (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ (1), (3) | Transceiver channel PLL power supply (left side) | GX, GS, GT | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GXBR}$ (1), (3) | Transceiver channel PLL power supply (right side) | GX, GS | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GTBR}$ | Transceiver channel PLL power supply (right side) | GT | 2.85 | 3.0 | 3.15 | V |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHIP\_R}$ | Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCR\_GXBL}$ (2) | Receiver analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

| Symbol | Description | Devices | Minimum (4) | Typical | Maximum (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCR\_GXBR}$ (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCR\_GTBR}$ | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCT\_GXBL}$ (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GXBR}$ (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GTBR}$ | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCL\_GTBR}$ | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

**Notes to Table 7:**

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements**

| Conditions | Core Speed Grade | VCCR_GXB & VCCT_GXB (2) | VCCA_GXB | VCCH_GXB | Unit |
|---|---|---|---|---|---|
| If BOTH of the following conditions are true:<br>■ Data rate > 10.3 Gbps.<br>■ DFE is used. | All | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true (1):<br>■ ATX PLL is used.<br>■ Data rate > 6.5Gbps.<br>■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | All | 1.0 | | | |
| If ALL of the following conditions are true:<br>■ ATX PLL is not used.<br>■ Data rate ≤ 6.5Gbps.<br>■ DFE, AEQ, and EyeQ are not used. | C1, C2, I2, and I3YY | 0.90 | 2.5 | | |
| | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85 | 2.5 | | |

**Notes to Table 8:**

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices (1)**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

**Note to Table 9:**

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 1 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 2 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 50-Ω $R_S$ | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination with calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω $R_S$ | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | $V_{CCIO}$ = 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 50-Ω $R_T$ | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 V | –10 to +40 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω $R_T$ | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 V | –10 to +40 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 60-Ω and 120-Ω $R_T$ | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | $V_{CCIO}$ = 1.2 | –10 to +40 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 25-Ω $R_{S\_left\_shift}$ | Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

**Note to Table 11:**

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)**

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 25-Ω R, 50-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.0 and 2.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |

**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCPD}$ = 2.5 V | ±25 | ±25 | ±25 | ±25 | % |

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

**Equation 1. OCT Variation Without Recalibration for Stratix V Devices** *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

**Notes to Equation 1:**

(1) The $R_{OCT}$ value shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
(2) $R_{SCAL}$ is the OCT resistance value at power-up.
(3) $\Delta T$ is the variation of temperature with respect to the temperature at power-up.
(4) $\Delta V$ is the variation of voltage with respect to the $V_{CCIO}$ at power-up.
(5) dR/dT is the percentage change of $R_{SCAL}$ with temperature.
(6) dR/dV is the percentage change of $R_{SCAL}$ with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)** *(1)*

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|---|---|---|---|---|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.0297 | %/mV |
| | | 2.5 | 0.0344 | |
| | | 1.8 | 0.0499 | |
| | | 1.5 | 0.0744 | |
| | | 1.2 | 0.1241 | |

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) (1)**

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|---|---|---|---|---|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/°C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

**Note to Table 13:**

(1) Valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0° to 85°C.

## Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on the top and bottom I/O pins | 6 | pF |
| $C_{IOLR}$ | Input capacitance on the left and right I/O pins | 6 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

## Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

| Symbol | Description | Maximum |
|---|---|---|
| $I_{IOPIN\ (DC)}$ | DC current per I/O pin | 300 µA |
| $I_{IOPIN\ (AC)}$ | AC current per I/O pin | 8 mA (1) |
| $I_{XCVR\text{-}TX\ (DC)}$ | DC current per transceiver transmitter pin | 100 mA |
| $I_{XCVR\text{-}RX\ (DC)}$ | DC current per transceiver receiver pin | 50 mA |

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

## Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices** *(1), (2)*

| Symbol | Description | $V_{CCIO}$ Conditions (V) *(3)* | Value *(4)* | Unit |
|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

**Notes to Table 16:**

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 66. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | — | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 16 | –16 |
| SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75* $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75* $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1* $V_{CCIO}$ | 0.9* $V_{CCIO}$ | — | — |

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.2 | — | $V_{CCIO}/2$ + 0.2 | 0.62 | $V_{CCIO}$ + 0.6 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 | 0.5 | $V_{CCIO}$ + 0.6 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | *(1)* | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | *(1)* | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | *(1)* | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF}$ –0.15 | $V_{CCIO}/2$ | $V_{REF}$ + 0.15 | –0.30 | 0.30 |

**Note to Table 20:**

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5* $V_{CCIO}$ | — | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5*$V_{CCIO}$ – 0.12 | 0.5* $V_{CCIO}$ | 0.5*$V_{CCIO}$ + 0.12 | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.44 | 0.44 |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices** *(7)*

| I/O Standard | $V_{CCIO}$ (V) *(10)* | | | $V_{ID}$ (mV) *(8)* | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) *(6)* | | | $V_{OCM}$ (V) *(6)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. | | | | | | | | | | | | | | |
| 2.5 V LVDS *(1)* | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX} \leq$ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS *(5)* | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| RSDS (HIO) *(2)* | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) *(3)* | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL *(4), (9)* | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Notes to Table 22:**

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110\ \Omega$ .

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

# Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

## Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 1 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Input Reference Clock Frequency (CMU PLL) (8) | — | 40 | — | 710 | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) (8) | — | 100 | — | 710 | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal (26) | — | — | 400 | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal (26) | — | — | 400 | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express® (PCIe®) | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 2 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | — | 0 to –0.5 | — | — | 0 to –0.5 | — | % |
| On-chip termination resistors (21) | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ (5) | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) (3) | Dedicated reference clock pin | 1050/1000/900/850 (2) | | | 1050/1000/900/850 (2) | | | 1050/1000/900/850 (2) | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 (4) | | | 1.0/0.9/0.85 (4) | | | 1.0/0.9/0.85 (4) | | | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) (20) | 100 Hz | — | — | -70 | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥1 MHz | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) (17) | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | — | — | 3 | ps (rms) |
| $R_{REF}$ (19) | — | — | 1800 ±1% | — | — | 1800 ±1% | — | — | 1800 ±1% | — | Ω |
| **Transceiver Clocks** | | | | | | | | | | | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | — | 100 or 125 | — | MHz |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 3 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| **Receiver** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) (9), (23) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) (9), (23) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Absolute $V_{MAX}$ for a receiver pin (5) | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration (22) | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration (18), (22) | $V_{CCR\_GXB}$ = 1.0 V/1.05 V ($V_{ICM}$ = 0.70 V) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR\_GXB}$ = 0.90 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR\_GXB}$ = 0.85 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins (6), (22), (27) | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 4 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors (21) | 85–Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100–Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120–Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC and DC coupled) | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V full bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V half bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V/1.05 V full bandwidth | — | 700 | — | — | 700 | — | — | 700 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | — | 750 | — | mV |
| $t_{LTR}$ (11) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ (12) | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$ (13) | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$ (14) | — | 15 | — | — | 15 | — | — | 15 | — | — | µs |
| Run Length | — | — | — | 200 | — | — | 200 | — | — | 200 | UI |
| Programmable equalization (AC Gain) (10) | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | — | — | 16 | dB |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 5 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 2 | — | — | 2 | — | — | 2 | — | dB |
| | DC Gain Setting = 2 | — | 4 | — | — | 4 | — | — | 4 | — | dB |
| | DC Gain Setting = 3 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| | DC Gain Setting = 4 | — | 8 | — | — | 8 | — | — | 8 | — | dB |
| **Transmitter** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Rise time (7) | 20% to 80% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Fall time (7) | 80% to 20% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | — | — | 120 | ps |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| **CMU PLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 7 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |

**Notes to Table 23:**

(1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the $V_{CCR\_GXB}$ power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

(4) This supply follows VCCR_GXB.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(8) The input reference clock frequency options depend on the data rate and the device speed grade.

(9) The line data rate may be limited by PCS-FPGA interface speed grade.

(10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(11) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(12) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(13) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(14) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(15) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(16) $t_{pll\_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(18) The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to 4 × (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

(19) For ES devices, $R_{REF}$ is 2000 Ω ±1%.

(20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(22) Refer to Figure 2.

(23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(24) I3YY devices can achieve data rates up to 10.3125 Gbps.

(25) When you use fPLL as a TXPLL of the transceiver.

(26) `REFCLK` performance requires to meet transmitter `REFCLK` phase noise specification.

(27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications** *(1)*

| Clock Network | ATX PLL | | | CMU PLL *(2)* | | | fPLL | | |
|---|---|---|---|---|---|---|---|---|---|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 *(3)* | 14.1 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 *(3)* | — | 14.1 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback *(4)* | — | 14.1 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

**Notes to Table 24:**

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate** *(1), (3)*

| Mode *(2)* | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 | 8.5 | 8.5 | 8.5 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.8 | 4.2 | 3.84 | 3.44 |
| Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

**Notes to Table 25:**

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 26 shows the approximate maximum data rate using the 10G PCS.

**Table 26. Stratix V 10G PCS Approximate Maximum Data Rate** *(1)*

| Mode *(2)* | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---|---|---|---|---|---|---|---|---|
| | | PCS Width | 64 | 66/67 | 50 | 40 | 64/66/67 | 32 |
| FIFO or Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 14.1 | 14.1 | 10.69 | 14.1 | 13.6 | 13.6 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 12.5 | 12.5 |
| | | C3, I3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps | | | | | |
| | | C3, I3, I3L core speed grade | | | | | | |
| | | C4, I4 core speed grade | | | | | | |
| | | I3YY core speed grade | 10.3125 Gbps | | | | | |

**Notes to Table 26:**

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Table 27 shows the $V_{OD}$ settings for the GX channel.

**Table 27. Typical $V_{OD}$ Setting for GX Channel, TX Termination = 100 Ω (2)**

| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| $V_{OD}$ differential peak to peak typical (3) | 0 (1) | 0 | 32 | 640 |
| | 1 (1) | 20 | 33 | 660 |
| | 2 (1) | 40 | 34 | 680 |
| | 3 (1) | 60 | 35 | 700 |
| | 4 (1) | 80 | 36 | 720 |
| | 5 (1) | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |
| | 15 | 300 | 47 | 940 |
| | 16 | 320 | 48 | 960 |
| | 17 | 340 | 49 | 980 |
| | 18 | 360 | 50 | 1000 |
| | 19 | 380 | 51 | 1020 |
| | 20 | 400 | 52 | 1040 |
| | 21 | 420 | 53 | 1060 |
| | 22 | 440 | 54 | 1080 |
| | 23 | 460 | 55 | 1100 |
| | 24 | 480 | 56 | 1120 |
| | 25 | 500 | 57 | 1140 |
| | 26 | 520 | 58 | 1160 |
| | 27 | 540 | 59 | 1180 |
| | 28 | 560 | 60 | 1200 |
| | 29 | 580 | 61 | 1220 |
| | 30 | 600 | 62 | 1240 |
| | 31 | 620 | 63 | 1260 |

**Note to Table 27:**

(1) If TX termination resistance = 100Ω, this VOD setting is illegal.

(2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.

(3) Refer to Figure 2.

Figure 2 shows the differential transmitter output waveform.

**Figure 2. Differential Transmitter Output Waveform**

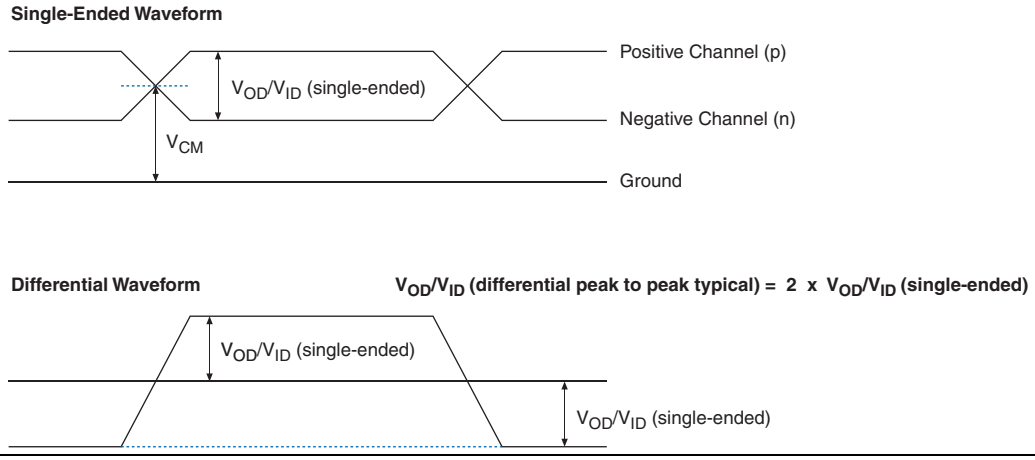
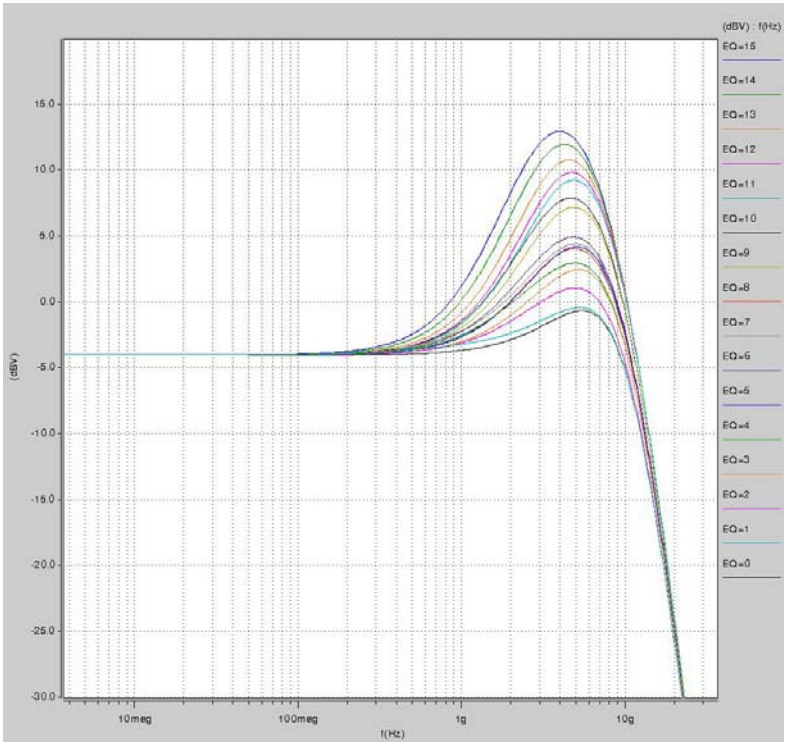



Figure 3 shows the Stratix V AC gain curves for GX channels.

**Figure 3. AC Gain Curves for GX Channels (full bandwidth)**




Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Input Reference Clock Frequency (CMU PLL) (6) | — | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) (6) | — | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | 20% to 80% | — | — | 400 | — | — | 400 | ps |
| Fall time | 80% to 20% | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | — | 0 to –0.5 | — | % |
| On-chip termination resistors (19) | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ (3) | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) | Dedicated reference clock pin | 1050/1000 (2) | | | 1050/1000 (2) | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 (22) | | | 1.0/0.9/0.85 (22) | | | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5)** *(1)*

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter REFCLK Phase Noise (622 MHz) *(18)* | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | |
| | 10 kHz | — | — | -100 | — | — | -100 | |
| | 100 kHz | — | — | -110 | — | — | -110 | |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | |
| Transmitter REFCLK Phase Jitter (100 MHz) *(15)* | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| RREF *(17)* | — | — | 1800 ± 1% | — | — | 1800 ± 1% | — | Ω |
| **Transceiver Clocks** | | | | | | | | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (`mgmt_clk_clk`) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |
| **Receiver** | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Data rate (Standard PCS) *(21)* | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) *(21)* | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Absolute $V_{MAX}$ for a receiver pin *(3)* | GT channels | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | GT channels | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration *(20)* | GT channels | — | — | 1.6 | — | — | 1.6 | V |
| | GX channels | *(8)* | | | | | | |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration *(16)*, *(20)* | GT channels $V_{CCR\_GTB}$ = 1.05 V ($V_{ICM}$ = 0.65 V) | — | — | 2.2 | — | — | 2.2 | V |
| | GX channels | *(8)* | | | | | | |
| Minimum differential eye opening at receiver serial input pins *(4)*, *(20)* | GT channels | 200 | — | — | 200 | — | — | mV |
| | GX channels | *(8)* | | | | | | |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors (7) | GT channels | — | 100 | — | — | 100 | — | Ω |
| Differential on-chip termination resistors for GX channels (19) | 85-Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100-Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120-Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC coupled) | GT channels | — | 650 | — | — | 650 | — | mV |
| VICM (AC and DC coupled) for GX Channels | VCCR_GXB = 0.85 V or 0.9 V | — | 600 | — | — | 600 | — | mV |
| | VCCR_GXB = 1.0 V full bandwidth | — | 700 | — | — | 700 | — | mV |
| | VCCR_GXB = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | mV |
| $t_{LTR}$ (9) | — | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ (10) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$ (11) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$ (12) | — | 15 | — | — | 15 | — | — | µs |
| Run Length | GT channels | — | — | 72 | — | — | 72 | CID |
| | GX channels | (8) | | | | | | |
| CDR PPM | GT channels | — | — | 1000 | — | — | 1000 | ± PPM |
| | GX channels | (8) | | | | | | |
| Programmable equalization (AC Gain) (5) | GT channels | — | — | 14 | — | — | 14 | dB |
| | GX channels | (8) | | | | | | |
| Programmable DC gain (6) | GT channels | — | — | 7.5 | — | — | 7.5 | dB |
| | GX channels | (8) | | | | | | |
| Differential on-chip termination resistors (7) | GT channels | — | 100 | — | — | 100 | — | Ω |
| **Transmitter** | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | |
| Data rate (Standard PCS) | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5)** *(1)*

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Differential on-chip termination resistors | GT channels | — | 100 | — | — | 100 | — | Ω |
| | GX channels | *(8)* | | | | | | |
| $V_{OCM}$ (AC coupled) | GT channels | — | 500 | — | — | 500 | — | mV |
| | GX channels | *(8)* | | | | | | |
| Rise/Fall time | GT channels | — | 15 | — | — | 15 | — | ps |
| | GX channels | *(8)* | | | | | | |
| Intra-differential pair skew | GX channels | *(8)* | | | | | | |
| Intra-transceiver block transmitter channel-to-channel skew | GX channels | *(8)* | | | | | | |
| Inter-transceiver block transmitter channel-to-channel skew | GX channels | *(8)* | | | | | | |
| **CMU PLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 8500 | Mbps |
| $t_{pll\_powerdown}$ *(13)* | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ *(14)* | — | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | |
| Supported Data Rate Range for GX Channels | VCO post-divider L=2 | 8000 | — | 12500 | 8000 | — | 8500 | Mbps |
| | L=4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| Supported Data Rate Range for GT Channels | VCO post-divider L=2 | 9800 | — | 14025 | 9800 | — | 12890 | Mbps |
| $t_{pll\_powerdown}$ *(13)* | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ *(14)* | — | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3.125 *(23)* | 600 | — | 3250/ 3.125 *(23)* | Mbps |
| $t_{pll\_powerdown}$ *(13)* | — | 1 | — | — | 1 | — | — | µs |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |

**Notes to Table 28:**

(1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(6) Refer to Figure 6 for the GT channel DC gain curves.

(7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.

(9) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(10) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(11) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(12) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(13) `tpll_powerdown` is the PLL powerdown minimum pulse width.

(14) `tpll_lock` is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(16) The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to 4 × (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

(17) For ES devices, RREF is 2000 Ω ±1%.

(18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(20) Refer to Figure 4.

(21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(22) This supply follows VCCR_GXB for both GX and GT channels.

(23) When you use fPLL as a TXPLL of the transceiver.

Table 29 shows the $V_{OD}$ settings for the GT channel.

**Table 29. Typical $V_{OD}$ Setting for GT Channel, TX Termination = 100 Ω**

| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|
| $V_{OD}$ differential peak to peak typical (1) | 0 | 0 |
| | 1 | 200 |
| | 2 | 400 |
| | 3 | 600 |
| | 4 | 800 |
| | 5 | 1000 |

**Note:**

(1) Refer to Figure 4.

Figure 4 shows the differential transmitter output waveform.

**Figure 4. Differential Transmitter/Receiver Output/Input Waveform**

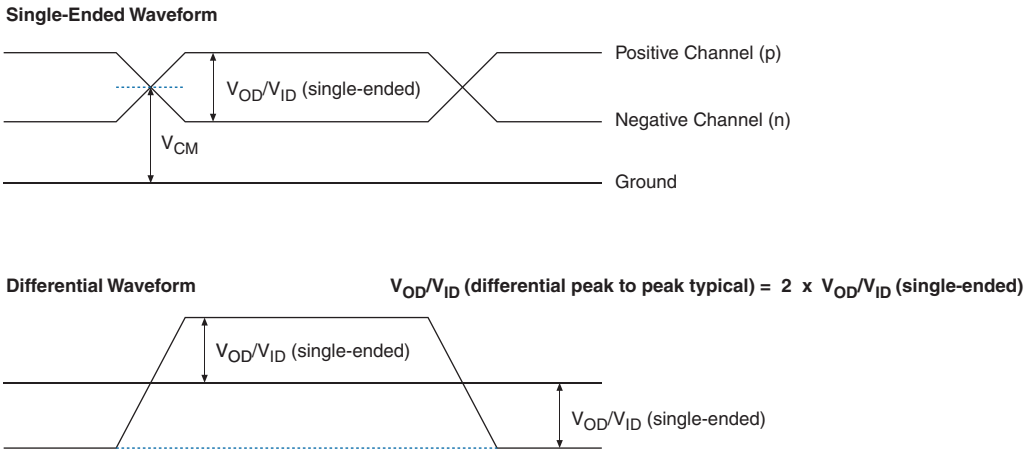



Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5. AC Gain Curves for GT Channels**

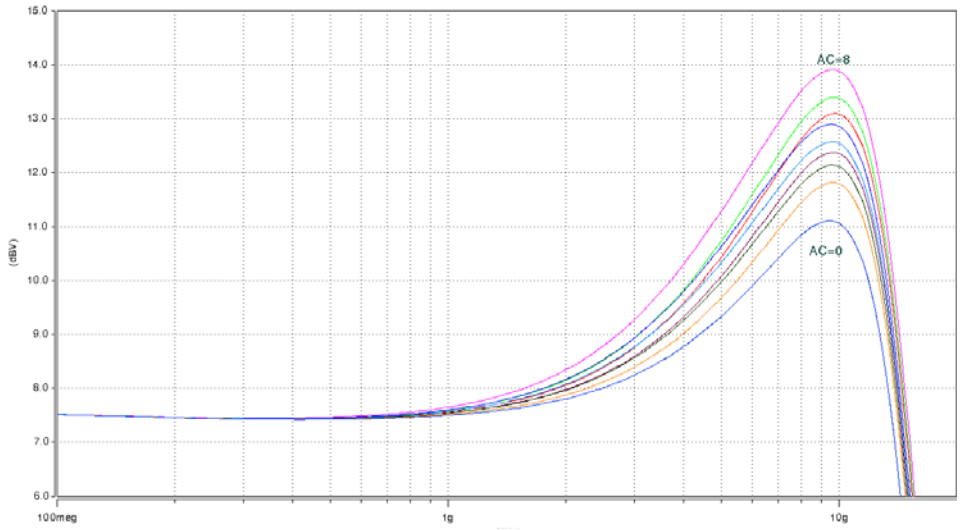
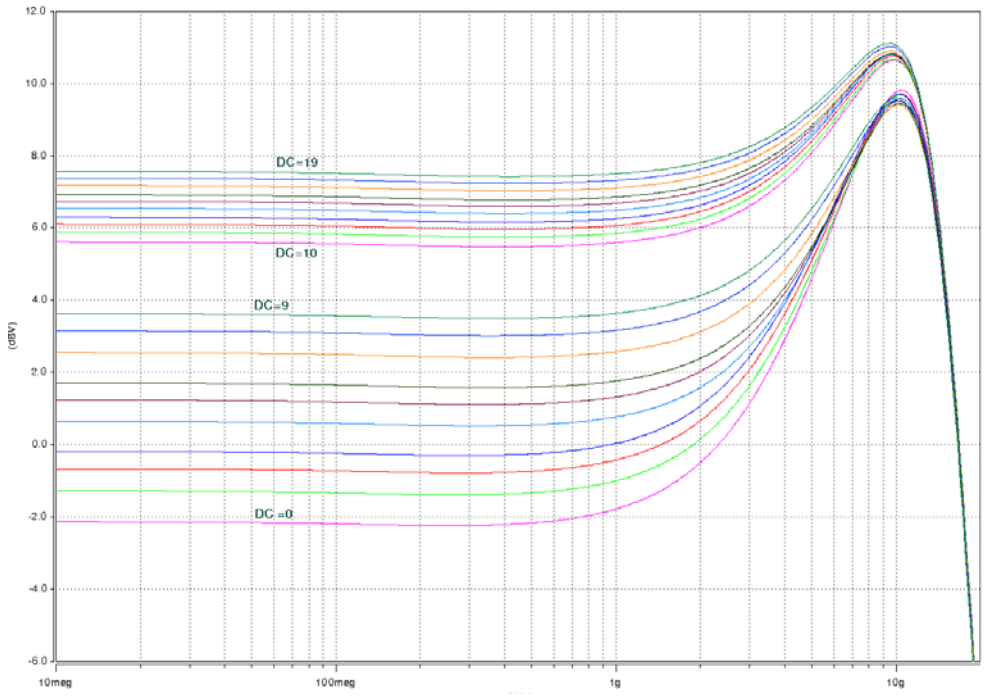


Figure 6 shows the Stratix V DC gain curves for GT channels.

**Figure 6. DC Gain Curves for GT Channels**




## Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

# Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

## Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices** *(1)*

| Symbol | Performance | | | Unit |
|---|---|---|---|---|
| | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 | |
| Global and Regional Clock | 717 | 650 | 580 | MHz |
| Periphery Clock | 550 | 500 | 500 | MHz |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C3, I3, I3L, and I3YY speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C4, I4 speed grades) | 5 | — | 650 (1) | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| $f_{VCO}$ (9) | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C3, I3, I3L, I3YY speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grades) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades) | — | — | 717 (2) | MHz |
| | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades) | — | — | 650 (2) | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grades) | — | — | 580 (2) | MHz |
| $f_{OUT\_EXT}$ | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades) | — | — | 800 (2) | MHz |
| | Output frequency for an external clock output (C3, I3, I3L speed grades) | — | — | 667 (2) | MHz |
| | Output frequency for an external clock output (C4, I4 speed grades) | — | — | 553 (2) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to **50%**) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic Configuration Clock used for `mgmt_clk` and `scanclk` | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from the end-of-device configuration or deassertion of `areset` | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth (7) | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |

**Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{INCCJ}$ (3), (4) | Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz) | –750 | — | +750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 (1) | ps (p-p) |
| | Period Jitter for dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 (1) | mUI (p-p) |
| $t_{FOUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ (5) | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ\_DC}$ (5) | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)+ | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTPJ\_IO}$ (5), (8) | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{FOUTPJ\_IO}$ (5), (8), (11) | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ (5), (8) | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{FOUTCCJ\_IO}$ (5), (8), (11) | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ (5), (6) | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for a duration of 100 µs | — | — | ±10 | % |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |

**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{RES}$ | Resolution of VCO frequency ($f_{INPFD}$ = 100 MHz) | 390625 | 5.96 | 0.023 | Hz |

**Notes to Table 31:**

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.

(4) $f_{REF}$ is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.

(9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post divider value. Therefore, if the VCO post divider value is 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(10) This specification only covers fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05 - 0.95 must be ≥ 1000 MHz, while $f_{VCO}$ for fractional value range 0.20 - 0.80 must be ≥ 1200 MHz.

(11) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05-0.95 must be ≥ 1000 MHz.

(12) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

| Mode | Peformance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| **Modes using one DSP** | | | | | | | | |
| Three 9 x 9 | 600 | 600 | 600 | 480 | 480 | 420 | 420 | MHz |
| One 18 x 18 | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| Two partial 18 x 18 (or 16 x 16) | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| One 27 x 27 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of two 18 x 18(One sum of 2 16 x 16) | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of square | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 18 x 18 plus 36 (a x b) + c | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| **Modes using two DSPs** | | | | | | | | |
| Three 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of four 18 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One sum of two 27 x 27 | 465 | 465 | 450 | 380 | 380 | 300 | 290 | MHz |
| One sum of two 36 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One complex 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 36 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)**

| Mode | Peformance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| **Modes using Three DSPs** | | | | | | | | |
| One complex 18 x 25 | 425 | 425 | 415 | 340 | 340 | 275 | 265 | MHz |
| **Modes using Four DSPs** | | | | | | | | |
| One complex 27 x 27 | 465 | 465 | 465 | 380 | 380 | 300 | 290 | MHz |

## Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

**Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 1 of 2)**

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| MLAB | Single port, all supported widths | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x32/x64 depth | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x16 depth (3) | 0 | 1 | 675 | 675 | 533 | 400 | 675 | 533 | 400 | MHz |
| | ROM, all supported widths | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |

**Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 2 of 2)**

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 0 | 1 | 525 | 525 | 455 | 400 | 525 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 450 | 450 | 400 | 350 | 450 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |

**Notes to Table 33:**

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in $F_{MAX}$.

(3) The $F_{MAX}$ specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

## Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

**Table 34. Internal Temperature Sensing Diode Specification**

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time (1) | Resolution | Minimum Resolution with no Missing Codes |
|---|---|---|---|---|---|---|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 KHz | < 100 ms | 8 bits | 8 bits |

**Note to Table 34:**

(1) For more details about the temperature sensing operations, refer to the *Intel FPGA Temperature Sensor IP Core User Guide*.

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

**Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices (Part 1 of 2)**

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $I_{bias}$, diode source current | 8 | — | 200 | µA |
| $V_{bias}$, voltage across diode | 0.3 | — | 0.9 | V |

**Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices (Part 2 of 2)**

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

## Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK\_in}$ (input clock frequency) True Differential I/O Standards | Clock boost factor W = 1 to 40 (4) | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) Single Ended I/O Standards (3) | Clock boost factor W = 1 to 40 (4) | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor W = 1 to 40 (4) | 5 | — | 520 | 5 | — | 520 | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{HSCLK\_OUT}$ (output clock frequency) | — | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 (5) | 5 | — | 525 (5) | MHz |

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Transmitter** | | | | | | | | | | | | | | |
| True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 (9), (11), (12), (13), (14), (15), (16) | (6) | — | 1600 | (6) | — | 1434 | (6) | — | 1250 | (6) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16) | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - $f_{HSDR}$ (data rate) (10) | SERDES factor J = 4 to 10 (17) | (6) | — | 1100 | (6) | — | 1100 | (6) | — | 840 | (6) | — | 840 | Mbps |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{DUTY}$ | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{RISE}$ & $t_{FALL}$ | True Differential I/O Standards | — | — | 160 | — | — | 160 | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 250 | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| **Receiver** | | | | | | | | | | | | | | |
| True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16) | 150 | — | 1434 | 150 | — | 1434 | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16) | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| **DPA Mode** | | | | | | | | | | | | | | |
| DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| **Soft CDR mode** | | | | | | | | | | | | | | |
| Soft-CDR PPM tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ± PPM |
| **Non DPA Mode** | | | | | | | | | | | | | | |
| Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |

**Notes to Table 36:**

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

**Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled**

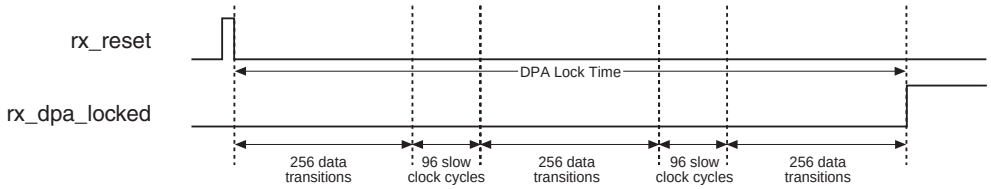



Table 37 lists the DPA lock time specifications for Stratix V devices.

**Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only** *(1), (2), (3)*

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions *(4)* | Maximum |
|---|---|---|---|---|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

**Notes to Table 37:**

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in this table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

**Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps**

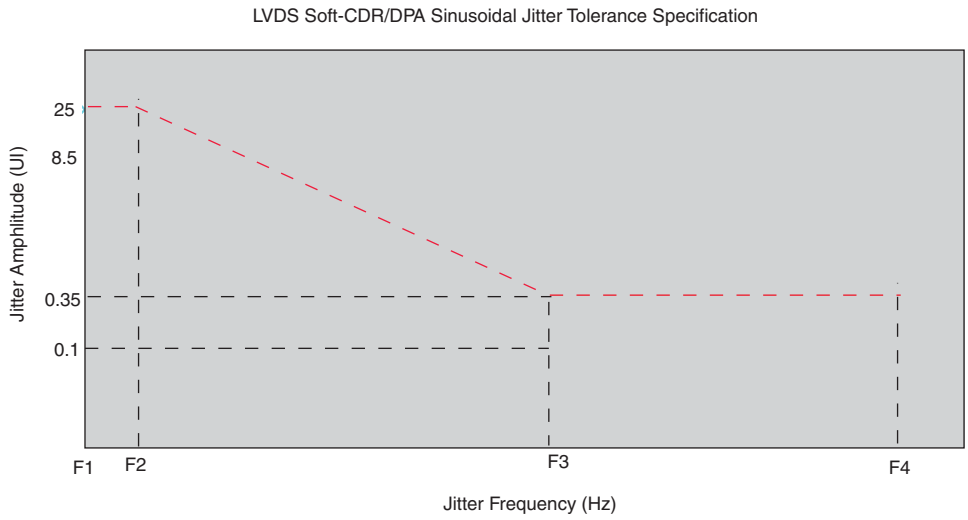
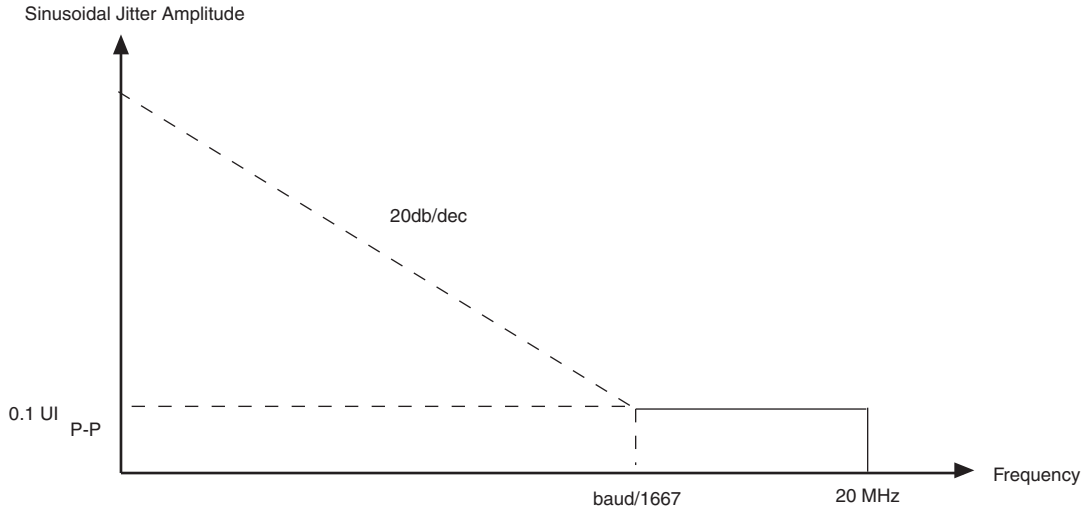


**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps**

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps**




## DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices** *(1)*

| C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---|---|---|---|---|
| 300-933 | 300-933 | 300-890 | 300-890 | MHz |

**Note to Table 39:**

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices** *(1), (2)* **(Part 1 of 2)**

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C1 | 8 | 14 | ps |
| C2, C2L, I2, I2L | 8 | 14 | ps |
| C3,I3, I3L, I3YY | 8 | 15 | ps |

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 2 of 2)**

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C4,I4 | 8 | 16 | ps |

**Notes to Table 40:**

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

**Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS\_PSERR}$) for Stratix V Devices (1)**

| Number of DQS Delay Buffers | C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---|---|---|---|---|---|
| 1 | 28 | 28 | 30 | 32 | ps |
| 2 | 56 | 56 | 60 | 64 | ps |
| 3 | 84 | 84 | 90 | 96 | ps |
| 4 | 112 | 112 | 120 | 128 | ps |

**Notes to Table 41:**

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is ±78 ps or ±39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 1 of 2) (2), (3)**

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | –50 | 50 | –50 | 50 | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –100 | 100 | –100 | 100 | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –50 | 50 | –50 | 50 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | –75 | 75 | –75 | 75 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –150 | 150 | –150 | 150 | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –75 | 75 | –75 | 75 | –90 | 90 | –90 | 90 | ps |

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)**

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| PHY Clock | Clock period jitter | $t_{JIT(per)}$ | –25 | 25 | –25 | 25 | –30 | 30 | –35 | 35 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –50 | 50 | –50 | 50 | –60 | 60 | –70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –37.5 | 37.5 | –37.5 | 37.5 | –45 | 45 | –56 | 56 | ps |

**Notes to Table 42:**

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

## OCT Calibration Block Specifications

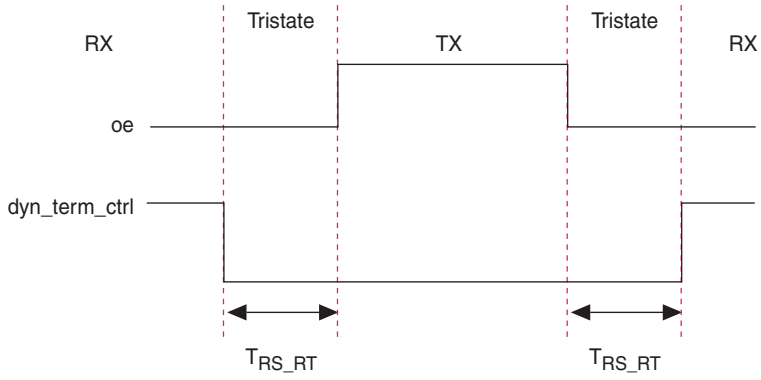
Table 43 lists the OCT calibration block specifications for Stratix V devices.

**Table 43. OCT Calibration Block Specifications for Stratix V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by the OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for the OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS\_RT}$ | Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10) | — | 2.5 | — | ns |

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

**Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals**



### Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

**Table 44. Worst-Case DCD on Stratix V I/O Pins** *(1)*

| Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Note to Table 44:**

(1) The DCD numbers do not cover the core clock network.

# Configuration Specification

## POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

**Table 45. Fast and Standard POR Delay Specification** *(1)*

| POR Delay | Minimum | Maximum |
|---|---|---|
| Fast | 4 ms | 12 ms |
| Standard | 100 ms | 300 ms |

**Note to Table 45:**

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period *(2)* | 30 | — | ns |
| $t_{JCP}$ | TCK clock period *(2)* | 167 | — | ns |
| $t_{JCH}$ | TCK clock high time *(2)* | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time *(2)* | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 11 (1) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 (1) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 (1) | ns |

**Notes to Table 46:**

(1) A 1 ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 12 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V GX | 5SGXA3 | H35, F40, F35 (2) | 213,798,880 | 562,392 |
| | | H29, F35 (3) | 137,598,880 | 564,504 |
| | 5SGXA4 | — | 213,798,880 | 563,672 |
| | 5SGXA5 | — | 269,979,008 | 562,392 |
| | 5SGXA7 | — | 269,979,008 | 562,392 |
| | 5SGXA9 | — | 342,742,976 | 700,888 |
| | 5SGXAB | — | 342,742,976 | 700,888 |
| | 5SGXB5 | — | 270,528,640 | 584,344 |
| | 5SGXB6 | — | 270,528,640 | 584,344 |
| | 5SGXB9 | — | 342,742,976 | 700,888 |
| | 5SGXBB | — | 342,742,976 | 700,888 |
| Stratix V GT | 5SGTC5 | — | 269,979,008 | 562,392 |
| | 5SGTC7 | — | 269,979,008 | 562,392 |
| Stratix V GS | 5SGSD3 | — | 137,598,880 | 564,504 |
| | 5SGSD4 | F1517 | 213,798,880 | 563,672 |
| | | — | 137,598,880 | 564,504 |
| | 5SGSD5 | — | 213,798,880 | 563,672 |
| | 5SGSD6 | — | 293,441,888 | 565,528 |
| | 5SGSD8 | — | 293,441,888 | 565,528 |

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V E (1) | 5SEE9 | — | 342,742,976 | 700,888 |
| | 5SEEB | — | 342,742,976 | 700,888 |

**Notes to Table 47:**

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
(2) 36-transceiver devices.
(3) 24-transceiver devices.
(4) File size for the periphery image.
(5) The IOCSR **.rbf** size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (**.hex**) or tabular text file (**.ttf**) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

**Notes to Table 48:**

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

## DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[] ratio for each combination.

**Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

**Table 49. DCLK-to-DATA[] Ratio (1) (Part 2 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×32 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 4 |
| | Enabled | Disabled | 8 |
| | Enabled | Enabled | 8 |

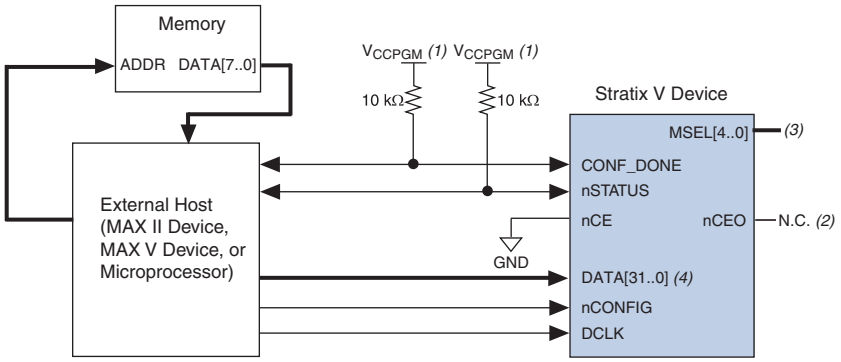
**Note to Table 49:**

(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

**Figure 11. Single Device FPP Configuration Using an External Host**




**Notes to Figure 11:**

(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. $V_{CCPGM}$ must be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with $V_{CCPGM}$.

(2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.

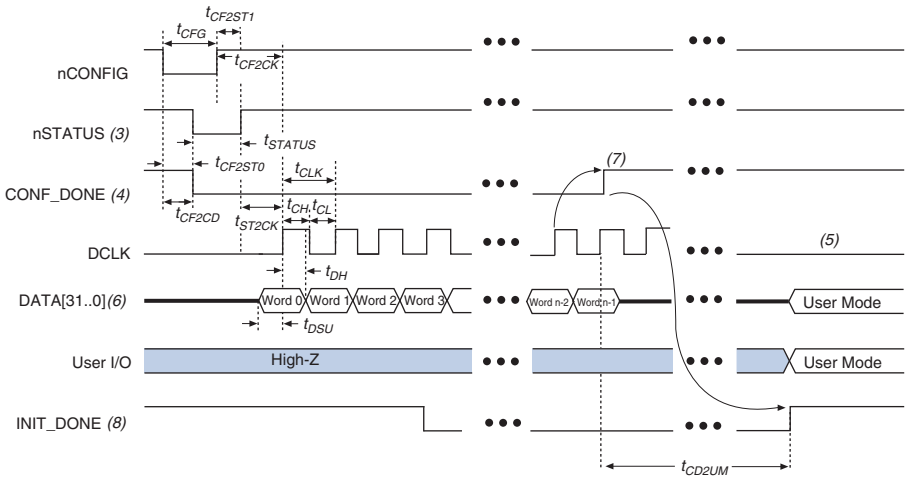
(3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(4) If you use FPP ×8, use DATA[7..0]. If you use FPP ×16, use DATA[15..0].

## FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.

**Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1** *(1), (2)*




**Notes to Figure 12:**

(1) Use this timing waveform when the DCLK-to-DATA[] ratio is 1.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.

(4) After power-up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.

(6) For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

**Table 50. FPP Timing Parameters for Stratix V Devices** *(1)*

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 *(2)* | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 *(3)* | µs |
| $t_{CF2CK}$ *(6)* | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ *(6)* | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode *(4)* | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) *(5)* | — | — |

**Notes to Table 50:**

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

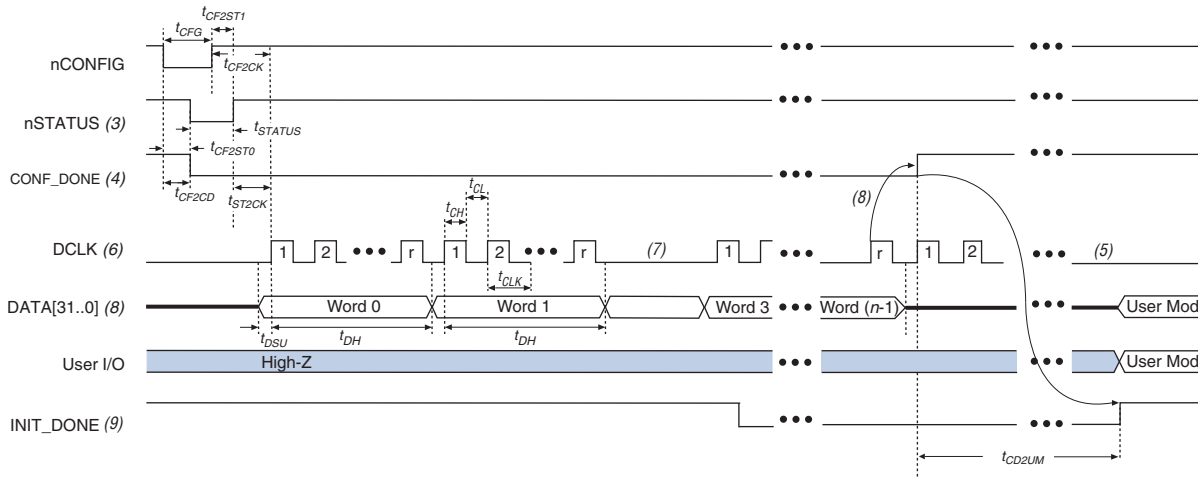
(5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(6) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

## FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

**Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1** *(1), (2)*




**Notes to Figure 13:**

(1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.

(4) After power-up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.

(7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.

(8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1** *(1)*

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 *(2)* | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 *(2)* | µs |
| $t_{CF2CK}$ *(5)* | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ *(5)* | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | N–1/$f_{DCLK}$ *(5)* | — | s |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode *(3)* | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) *(4)* | — | — |

**Notes to Table 51:**

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(5) N is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.

(6) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

## Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

**Table 52. DCLK Frequency Specification in the AS Configuration Scheme (1), (2)**

| Minimum | Typical | Maximum | Unit |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |
| 10.6 | 15.7 | 25.0 | MHz |
| 21.3 | 31.4 | 50.0 | MHz |
| 42.6 | 62.9 | 100.0 | MHz |

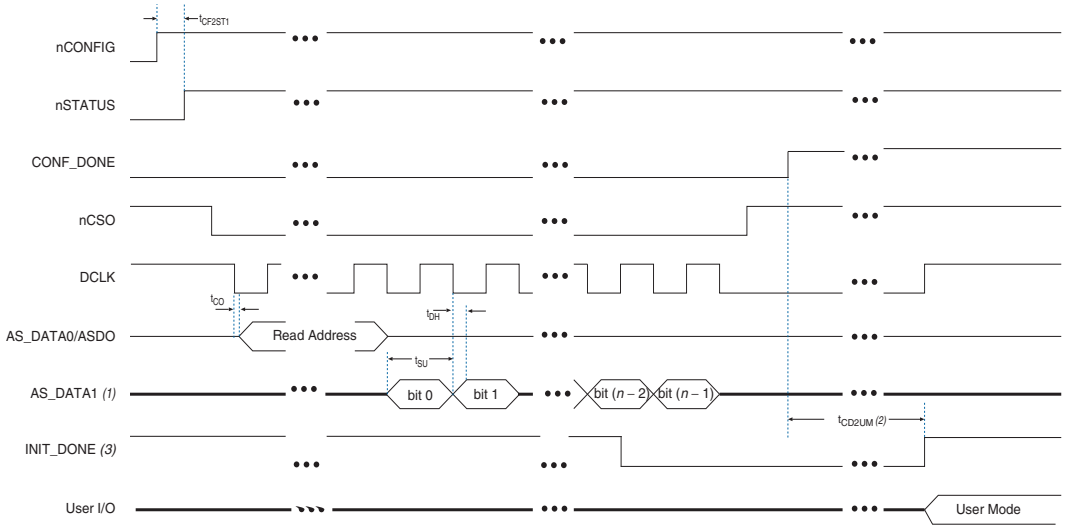
**Notes to Table 52:**

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

**Figure 14. AS Configuration Timing**




**Notes to Figure 14:**

(1) If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.

(2) The initialization clock can be from internal oscillator or CLKUSR pin.

(3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 1 of 2)**

| Symbol | Parameter | Condition | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $t_{CO}$ (3) | DCLK falling edge to AS_DATA0/ASDO output | — | — | 2 | ns |
| $t_{SU}$ (4) | Data setup time before falling edge on DCLK | — | 1.5 | — | ns |

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 2 of 2)**

| Symbol | Parameter | Condition | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| $t_{DH}$ (4) | Data hold time after falling edge on DCLK | –1 speed grade | 2.9 | — | ns |
| | | –2 speed grade | 3.4 | — | ns |
| | | –3 speed grade | 3.7 | — | ns |
| | | –4 speed grade | 3.9 | — | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode (5) | — | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | — | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | — | $t_{CD2CU}$ + (8576 × CLKUSR period) | — | — |

**Notes to Table 53:**

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) $t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, and $t_{CF2ST1}$ timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) Load capacitance for DCLK = 6 pF and AS_DATA/ASDO = 8 pF. Intel recommends obtaining the $t_{CO}$ for a given link (including receiver, transmission lines, connectors, termination resistors, and other components) through IBIS or HSPICE simulation.

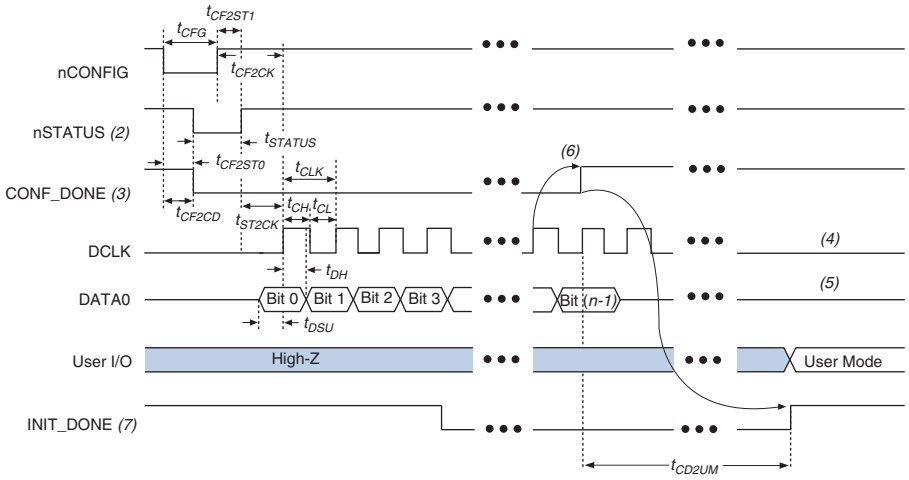
(4) To evaluate the data setup ($t_{SU}$) and data hold time ($t_{DH}$) slack on your board in order to ensure you are meeting the $t_{SU}$ and $t_{DH}$ requirement, Intel recommends following the guideline in the "Evaluating Data Setup and Hold Timing Slack" chapter in *AN822: Intel FPGA Configuration Device Migration Guideline*.

(5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

**Figure 15. PS Configuration Timing Waveform** *(1)*




**Notes to Figure 15:**

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.

(3) After power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

(6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

**Table 54. PS Timing Parameters for Stratix V Devices (Part 1 of 2)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 *(1)* | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 *(2)* | µs |
| $t_{CF2CK}$ *(5)* | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ *(5)* | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |

**Table 54. PS Timing Parameters for Stratix V Devices (Part 2 of 2)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode (3) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (4) | — | — |

**Notes to Table 54:**

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

## Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

**Table 55. Initialization Clock Source Option and the Maximum Frequency**

| Initialization Clock Source | Configuration Schemes | Maximum Frequency | Minimum Number of Clock Cycles (1) |
|---|---|---|---|
| Internal Oscillator | AS, PS, FPP | 12.5 MHz | 8576 |
| CLKUSR | AS, PS, FPP (2) | 125 MHz | |
| DCLK | PS, FPP | 125 MHz | |

**Notes to Table 55:**

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

## Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

**Table 56. Remote System Upgrade Circuitry Timing Specifications (Part 1 of 2)**

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| $t_{RU\_nCONFIG}$ (1) | 250 | — | ns |

**Table 56. Remote System Upgrade Circuitry Timing Specifications (Part 2 of 2)**

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| $t_{RU\_nRSTIMER}$ (2) | 250 | — | ns |

**Notes to Table 56:**

(1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

**Table 57. 12.5-MHz Internal Oscillator Specifications**

| Minimum | Typical | Maximum | Units |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)**

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D1 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D2 | 32 | 0 | 0.230 | 0.244 | 0.415 | 0.415 | 0.459 | 0.503 | 0.417 | 0.456 | 0.500 | ns |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

**Notes to Table 58:**

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or falling edge delay | 0 (default) | ps |
| | | 25 | ps |
| | | 50 | ps |
| | | 75 | ps |

**Note to Table 59:**

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

# Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **A**<br>B<br>C | — | — |
| **D** | — | — |
| **E** | — | — |
| **F** | $f_{HSCLK}$ | Left and right PLL input clock frequency. |
| | $f_{HSDR}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| | $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |
| **G**<br>H<br>I | — | — |

**Table 60. Glossary (Part 2 of 4)**

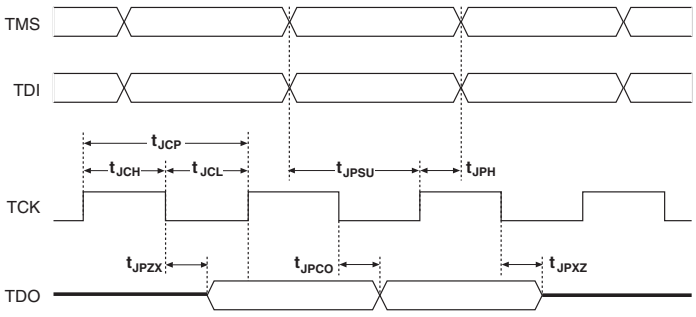
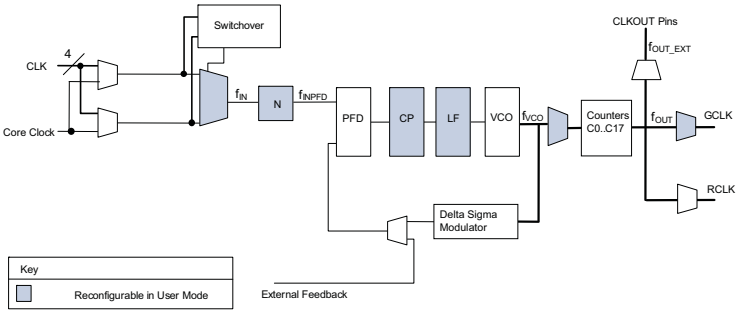
| Letter | Subject | Definitions |
|---|---|---|
| J | J | High-speed I/O block—Deserialization factor (width of parallel data bus). |
| J | JTAG Timing Specifications | JTAG Timing Specifications:<br>  |
| K<br>L<br>M<br>N<br>O | — | — |
| P | **PLL Specifications** | **Diagram of PLL Specifications** *(1)*<br>  <br>**Note:**<br>(1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs. |
| Q | — | — |
| R | $R_L$ | Receiver differential input discrete resistor (external to the Stratix V device). |

**Table 60. Glossary (Part 3 of 4)**

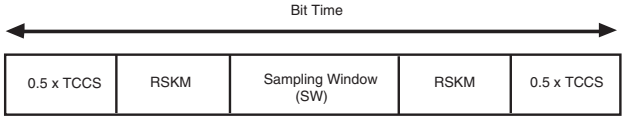
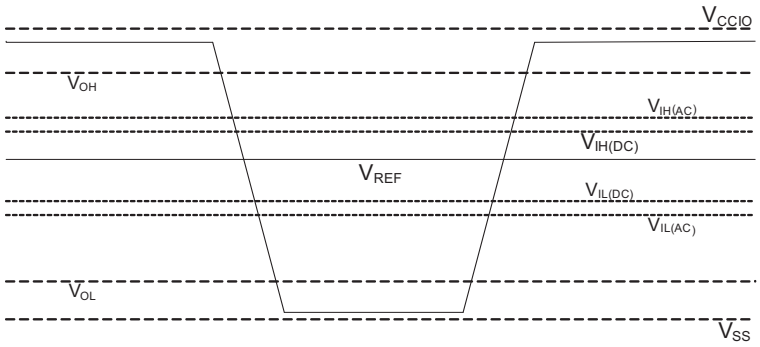
| Letter | Subject | Definitions |
|---|---|---|
| S | **SW (sampling window)** | Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:<br>  |
| | Single-ended voltage referenced I/O standard | The JEDEC standard for **SSTL** and **HSTL** I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:<br>*Single-Ended Voltage Referenced I/O Standard*<br>  |
| T | $t_C$ | High-speed receiver and transmitter input and output clock period. |
| | **TCCS (channel-to-channel-skew)** | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table). |
| | $t_{DUTY}$ | High-speed I/O block—Duty cycle on the high-speed transmitter output clock. |
| | | **Timing Unit Interval (TUI)**<br>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(receiver input clock frequency multiplication factor) = $t_C/w$) |
| | $t_{FALL}$ | Signal high-to-low transition time (80-20%) |
| | $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| | $t_{OUTPJ\_IO}$ | Period jitter on the general purpose I/O driven by a PLL. |
| | $t_{OUTPJ\_DC}$ | Period jitter on the dedicated clock output driven by a PLL. |
| | $t_{RISE}$ | Signal low-to-high transition time (20-80%) |
| U | — | — |

**Table 60. Glossary (Part 4 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| | $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage |
| | $V_{IH(DC)}$ | High-level DC input voltage |
| | $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage |
| | $V_{IL(DC)}$ | Low-level DC input voltage |
| | $V_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| | $V_{SWING}$ | Differential input voltage |
| | $V_X$ | Input differential cross point voltage |
| | $V_{OX}$ | Output differential cross point voltage |
| W | W | High-speed I/O block—clock boost factor |
| X<br>Y<br>Z | — | — |

# Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 4)**

| Date | Version | Changes |
|---|---|---|
| June 2019 | 4.1 | Added a note for Conversion Time in the “Internal Temperature Sensing Diode Specification” table. |
| January 2019 | 4.0 | ■ Changed "VCO post-scale counter K value" to "VCO post divider value" in the $f_{VCO}$ note in the “PLL Specifications for Stratix V Devices” table.<br>■ Updated the “AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices” table.<br>■ Updated $t_{DH}$ specifications. These specifications are applicable to the commercial and industrial grade devices.<br>■ Added note to $t_{CO}$, $t_{SU}$, and $t_{DH}$. |
| June 2018 | 3.9 | ■ Added the “Stratix V Device Overshoot Duration” figure. |

**Table 61. Document Revision History (Part 2 of 4)**

| Date | Version | Changes |
|---|---|---|
| April 2017 | 3.8 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “PS Timing Parameters for Stratix V Devices” table.<br>■ Changed the condition for 100-Ω $R_D$ in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | ■ Added the $V_{ID}$ minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table<br>■ Added the $I_{OUT}$ specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | ■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | ■ Changed the data rate specification for transceiver speed grade 3 in the following tables:<br>  ■ “Transceiver Specifications for Stratix V GX and GS Devices”<br>  ■ “Stratix V Standard PCS Approximate Maximum Date Rate”<br>  ■ “Stratix V 10G PCS Approximate Maximum Data Rate”<br>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the $t_{CO}$ maximum value in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table.<br>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |

**Table 61. Document Revision History (Part 3 of 4)**

| Date | Version | Changes |
|---|---|---|
| November 2014 | 3.3 | ■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.<br>■ Added the I3YY speed grade to the $V_{CC}$ description in Table 6.<br>■ Added the I3YY speed grade to $V_{CCHIP\_L}$, $V_{CCHIP\_R}$, $V_{CCHSSI\_L}$, and $V_{CCHSSI\_R}$ descriptions in Table 7.<br>■ Added 240-Ω to Table 11.<br>■ Changed CDR PPM tolerance in Table 23.<br>■ Added additional max data rate for fPLL in Table 23.<br>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.<br>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.<br>■ Changed CDR PPM tolerance in Table 28.<br>■ Added additional max data rate for fPLL in Table 28.<br>■ Changed the mode descriptions for MLAB and M20K in Table 33.<br>■ Changed the Max value of $f_{HSCLK\_OUT}$ for the C2, C2L, I2, I2L speed grades in Table 36.<br>■ Changed the frequency ranges for C1 and C2 in Table 39.<br>■ Changed the **.rbf** file sizes for 5SGSD6 and 5SGSD8 in Table 47.<br>■ Added note about nSTATUS to Table 50, Table 51, Table 54.<br>■ Changed the available settings in Table 58.<br>■ Changed the note in “Periphery Performance”.<br>■ Updated the “I/O Standard Specifications” section.<br>■ Updated the “Raw Binary File Size” section.<br>■ Updated the receiver voltage input range in Table 22.<br>■ Updated the max frequency for the LVDS clock network in Table 36.<br>■ Updated the DCLK note to Figure 11.<br>■ Updated Table 23 $VO_{CM}$ (DC Coupled) condition.<br>■ Updated Table 6 and Table 7.<br>■ Added the DCLK specification to Table 55.<br>■ Updated the notes for Table 47.<br>■ Updated the list of parameters for Table 56. |
| November 2013 | 3.2 | ■ Updated Table 28 |
| November 2013 | 3.1 | ■ Updated Table 33 |
| November 2013 | 3.0 | ■ Updated Table 23 and Table 28 |
| October 2013 | 2.9 | ■ Updated the “Transceiver Characterization” section |
| October 2013 | 2.8 | ■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59<br>■ Added Figure 1 and Figure 3<br>■ Added the “Transceiver Characterization” section<br>■ Removed all “Preliminary” designations. |

**Table 61. Document Revision History (Part 4 of 4)**

| Date | Version | Changes |
|---|---|---|
| May 2013 | 2.7 | ■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60<br>■ Added Table 24, Table 48<br>■ Updated Figure 9, Figure 10, Figure 11, Figure 12 |
| February 2013 | 2.6 | ■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46<br>■ Updated “Maximum Allowed Overshoot and Undershoot Voltage” |
| December 2012 | 2.5 | ■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35<br>■ Added Table 33<br>■ Added “Fast Passive Parallel Configuration Timing”<br>■ Added “Active Serial Configuration Timing”<br>■ Added “Passive Serial Configuration Timing”<br>■ Added “Remote System Upgrades”<br>■ Added “User Watchdog Internal Circuitry Timing Specification”<br>■ Added “Initialization”<br>■ Added “Raw Binary File Size” |
| June 2012 | 2.4 | ■ Added Figure 1, Figure 2, and Figure 3.<br>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27,Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.<br>■ Various edits throughout to fix bugs.<br>■ Changed title of document to *Stratix V Device Datasheet*.<br>■ Removed document from the Stratix V handbook and made it a separate document. |
| February 2012 | 2.3 | ■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31. |
| December 2011 | 2.2 | ■ Added Table 2–31.<br>■ Updated Table 2–28 and Table 2–34. |
| November 2011 | 2.1 | ■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.<br>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.<br>■ Various edits throughout to fix SPRs. |
| May 2011 | 2.0 | ■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.<br>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.<br>■ Chapter moved to Volume 1.<br>■ Minor text edits. |
| December 2010 | 1.1 | ■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.<br>■ Converted chapter to the new template.<br>■ Minor text edits. |
| July 2010 | 1.0 | Initial release. |

In Clear Electronics

WWW.IC-1000.COM

# THE DATASHEET OF FPGA


www.ic-1000.com info@ic-1000.com

+00852-56412601 +00852-56412601

Unit B，13/F，Shing Lee Commercial Building
No.8 Wing Kut Street，Central HK