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Introduction

Virtex®-7 T and XT FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices operate at $V_{CCINT} = 1.0V$ and are screened for lower maximum static power. The speed specification of a -2L device is the same as the -2 speed grade. The -2G speed grade is available in devices utilizing Stacked Silicon Interconnect (SSI) technology. The -2G speed grade supports 12.5 Gb/s GTX or 13.1 Gb/s GTH transceivers as well as the standard -2 speed grade specifications.

Virtex-7 T and XT FPGA DC and AC characteristics are specified in commercial, extended, industrial, and military temperature ranges. Except for the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1M speed grade military

device are the same as for a -1C speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found in:

- *7 Series FPGAs Overview* ([DS180](#))
- *Defense-Grade 7 Series FPGAs Overview* ([DS185](#))

This Virtex-7 T and XT FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

DC Characteristics

Table 1: Absolute Maximum Ratings⁽¹⁾

| Symbol | Description | Min | Max | Units |
|---------------------------------|---|-------|------------------|-------|
| FPGA Logic | | | | |
| V_{CCINT} | Internal supply voltage | -0.5 | 1.1 | V |
| V_{CCAUX} | Auxiliary supply voltage | -0.5 | 2.0 | V |
| V_{CCBRAM} | Supply voltage for the block RAM memories | -0.5 | 1.1 | V |
| V_{CCO} | Output drivers supply voltage for 3.3V HR I/O banks | -0.5 | 3.6 | V |
| | Output drivers supply voltage for 1.8V HP I/O banks | -0.5 | 2.0 | V |
| V_{CCAUX_IO} | Auxiliary supply voltage | -0.5 | 2.06 | V |
| V_{REF} | Input reference voltage | -0.5 | 2.0 | V |
| $V_{IN}^{(2)(3)(4)}$ | I/O input voltage for 3.3V HR I/O banks | -0.40 | $V_{CCO} + 0.55$ | V |
| | I/O input voltage for 1.8V HP I/O banks | -0.55 | $V_{CCO} + 0.55$ | V |
| | I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMD5_33 ⁽⁵⁾ | -0.40 | 2.625 | V |
| V_{CCBATT} | Key memory battery backup supply | -0.5 | 2.0 | V |
| GTX and GTH Transceivers | | | | |
| $V_{MGTAVCC}$ | Analog supply voltage for the GTX/GTH transmitter and receiver circuits | -0.5 | 1.1 | V |
| $V_{MGTAVTT}$ | Analog supply voltage for the GTX/GTH transmitter and receiver termination circuits | -0.5 | 1.32 | V |
| $V_{MGTVCCAUX}$ | Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX/GTH transceivers | -0.5 | 1.935 | V |
| $V_{MGTREFCLK}$ | GTX/GTH transceiver reference clock absolute input voltage | -0.5 | 1.32 | V |

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

| Symbol | Description | Min | Max | Units |
|----------------------------|--|------|------|-------|
| V _{MGTAVTTRCAL} | Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column | -0.5 | 1.32 | V |
| V _{IN} | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | -0.5 | 1.26 | V |
| I _{DCIN-FLOAT} | DC input current for receiver input pins DC coupled RX termination = floating | - | 14 | mA |
| I _{DCIN-MGTAVTT} | DC input current for receiver input pins DC coupled RX termination = V _{MGTAVTT} | - | 12 | mA |
| I _{DCIN-GND} | DC input current for receiver input pins DC coupled RX termination = GND | - | 6.5 | mA |
| I _{DCOUT-FLOAT} | DC output current for transmitter pins DC coupled RX termination = floating | - | 14 | mA |
| I _{DCOUT-MGTAVTT} | DC output current for transmitter pins DC coupled RX termination = V _{MGTAVTT} | - | 12 | mA |
| XADC | | | | |
| V _{CCADC} | XADC supply relative to GNDADC | -0.5 | 2.0 | V |
| V _{REFP} | XADC reference input relative to GNDADC | -0.5 | 2.0 | V |
| Temperature | | | | |
| T _{STG} | Storage temperature (ambient) | -65 | 150 | °C |
| T _{SOL} | Maximum soldering temperature for Pb/Sn component bodies ⁽⁶⁾ | - | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies ⁽⁶⁾ | - | +260 | °C |
| T _j | Maximum junction temperature ⁽⁶⁾ | - | +125 | °C |

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide (UG471)*.
- The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see [Table 4](#) and [Table 5](#).
- See [Table 10](#) for TMD5_33 specifications.
- For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification (UG475)*.

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

| Symbol | Description | Min | Typ | Max | Units |
|--------------------------------------|--|-------|------|------------------------|-------|
| FPGA Logic | | | | | |
| V _{CCINT} ⁽³⁾ | Internal supply voltage | 0.97 | 1.00 | 1.03 | V |
| | Internal supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical ⁽⁴⁾ . | 0.87 | 0.90 | 0.93 | V |
| V _{CCBRAM} ⁽³⁾ | Block RAM supply voltage | 0.97 | 1.00 | 1.03 | V |
| | Block RAM supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical ⁽⁴⁾ . | 0.87 | 0.90 | 1.03 | V |
| V _{CCAUX} | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| V _{CCO} ⁽⁵⁾⁽⁶⁾ | Supply voltage for 3.3V HR I/O banks | 1.14 | - | 3.465 | V |
| | Supply voltage for 1.8V HP I/O banks | 1.14 | - | 1.89 | V |
| V _{CCAUX_IO} ⁽⁷⁾ | Auxiliary supply voltage when set to 1.8V | 1.71 | 1.80 | 1.89 | V |
| | Auxiliary supply voltage when set to 2.0V | 1.94 | 2.00 | 2.06 | V |
| V _{IN} ⁽⁸⁾ | I/O input voltage | -0.20 | - | V _{CCO} + 0.2 | V |
| | I/O input voltage (when V _{CCO} = 3.3V) for V _{REF} and differential I/O standards except TMD5_33 ⁽⁹⁾ | -0.20 | - | 2.625 | V |
| I _{IN} ⁽¹⁰⁾ | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | - | - | 10 | mA |

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

| Symbol | Description | Min | Typ | Max | Units |
|---------------------------------|---|------|------|------|-------|
| $V_{CCBATT}^{(11)}$ | Battery voltage | 1.0 | – | 1.89 | V |
| GTX and GTH Transceivers | | | | | |
| $V_{MGTAVCC}^{(12)}$ | Analog supply voltage for the GTX/GTH transceiver QPLL frequency range ≤ 10.3125 GHz ⁽¹³⁾⁽¹⁴⁾ | 0.97 | 1.0 | 1.08 | V |
| | Analog supply voltage for the GTX/GTH transceiver QPLL frequency range > 10.3125 GHz | 1.02 | 1.05 | 1.08 | V |
| $V_{MGTAVTT}^{(12)}$ | Analog supply voltage for the GTX/GTH transmitter and receiver termination circuits | 1.17 | 1.2 | 1.23 | V |
| $V_{MGTVCCAUX}^{(12)}$ | Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers | 1.75 | 1.80 | 1.85 | V |
| $V_{MGTAVTTRCAL}^{(12)}$ | Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column | 1.17 | 1.2 | 1.23 | V |
| XADC | | | | | |
| V_{CCADC} | XADC supply relative to GNDADC | 1.71 | 1.80 | 1.89 | V |
| V_{REFP} | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| Temperature | | | | | |
| T_j | Junction temperature operating range for commercial (C) temperature devices | 0 | – | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | – | 100 | °C |
| | Junction temperature operating range for military (M) temperature devices | –55 | – | 125 | °C |

Notes:

- All voltages are relative to ground.
- For the design of the power distribution system, consult the *7 Series FPGAs PCB Design and Pin Planning Guide* ([UG483](#)).
- V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- For more information on the VID bit see the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)).
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HR I/O only), 3.3V (HR I/O only) at $\pm 5\%$.
- For more information, refer to the V_{CCAUX_IO} section of *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)).
- The lower absolute voltage specification always applies.
- See [Table 10](#) for TMD5_33 specifications.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .
- Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
- For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be $1.0V \pm 3\%$ for lower power consumption.
- For lower power consumption, $V_{MGTAVCC}$ should be $1.0V \pm 3\%$ over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

| Symbol | Description | Min | Typ ⁽¹⁾ | Max | Units |
|----------------|---|------|--------------------|-----|---------|
| V_{DRINT} | Data retention V_{CCINT} voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| V_{DRI} | Data retention V_{CCAUX} voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| I_{REF} | V_{REF} leakage current per pin | – | – | 15 | μA |
| I_L | Input or output leakage current per pin (sample-tested) | – | – | 15 | μA |
| $C_{IN}^{(2)}$ | Die input capacitance at the pad | – | – | 8 | pF |

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

| Symbol | Description | Min | Typ ⁽¹⁾ | Max | Units |
|-------------------------------------|--|-----|--------------------|-----|-------|
| I _{RPU} | Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 3.3V | 90 | – | 330 | μA |
| | Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 2.5V | 68 | – | 250 | μA |
| | Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.8V | 34 | – | 220 | μA |
| | Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.5V | 23 | – | 150 | μA |
| | Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.2V | 12 | – | 120 | μA |
| I _{RPD} | Pad pull-down (when selected) @ V _{IN} = 3.3V | 68 | – | 330 | μA |
| | Pad pull-down (when selected) @ V _{IN} = 1.8V | 45 | – | 180 | μA |
| I _{CCADC} | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| I _{BATT} ⁽³⁾ | Battery supply current | – | – | 150 | nA |
| R _{IN_TERM} ⁽⁴⁾ | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_40) | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_50) | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to V _{CCO} /2 (UNTUNED_SPLIT_60) | 44 | 60 | 83 | Ω |
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst-case process at 25°C. For the XC7VX1140T and XC7V2000T devices, multiply the value by the number of super-logic regions (SLRs) in the device.
4. Termination resistance to a V_{CCO}/2 level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾⁽²⁾

| AC Voltage Overshoot | % of UI @ –55°C to 125°C | AC Voltage Undershoot | % of UI @ –55°C to 125°C |
|-------------------------|--------------------------|-----------------------|--------------------------|
| V _{CCO} + 0.55 | 100 | –0.40 | 100 |
| | | –0.45 | 61.7 |
| | | –0.50 | 25.8 |
| | | –0.55 | 11.0 |
| V _{CCO} + 0.60 | 46.6 | –0.60 | 4.77 |
| V _{CCO} + 0.65 | 21.2 | –0.65 | 2.10 |
| V _{CCO} + 0.70 | 9.75 | –0.70 | 0.94 |
| V _{CCO} + 0.75 | 4.55 | –0.75 | 0.43 |
| V _{CCO} + 0.80 | 2.15 | –0.80 | 0.20 |
| V _{CCO} + 0.85 | 1.02 | –0.85 | 0.09 |
| V _{CCO} + 0.90 | 0.49 | –0.90 | 0.04 |
| V _{CCO} + 0.95 | 0.24 | –0.95 | 0.02 |

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below GND – 0.20V, must not exceed the values in this table.

Table 5: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks⁽¹⁾⁽²⁾

| AC Voltage Overshoot | % of UI @ -55°C to 125°C | AC Voltage Undershoot | % of UI @ -55°C to 125°C |
|----------------------|--------------------------|-----------------------|--------------------------|
| $V_{CCO} + 0.55$ | 100 | -0.55 | 100 |
| $V_{CCO} + 0.60$ | 50.0 ⁽³⁾ | -0.60 | 50.0 ⁽³⁾ |
| $V_{CCO} + 0.65$ | 50.0 ⁽³⁾ | -0.65 | 50.0 ⁽³⁾ |
| $V_{CCO} + 0.70$ | 47.0 | -0.70 | 50.0 ⁽³⁾ |
| $V_{CCO} + 0.75$ | 21.2 | -0.75 | 50.0 ⁽³⁾ |
| $V_{CCO} + 0.80$ | 9.71 | -0.80 | 50.0 ⁽³⁾ |
| $V_{CCO} + 0.85$ | 4.51 | -0.85 | 28.4 |
| $V_{CCO} + 0.90$ | 2.12 | -0.90 | 12.7 |
| $V_{CCO} + 0.95$ | 1.01 | -0.95 | 5.79 |

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO} + 0.20V$ or below $GND - 0.20V$, must not exceed the values in this table.
3. For UI lasting less than 20 μs .

Table 6: Typical Quiescent Supply Current

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|--------------|--------------------------------------|------------|-------------|------|------|------|------|------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| I_{CCINTQ} | Quiescent V_{CCINT} supply current | XC7V585T | 1483 | 1483 | 1483 | 1483 | 1483 | N/A | mA |
| | | XC7V2000T | N/A | 3756 | 3756 | 3756 | 3756 | N/A | mA |
| | | XC7VX330T | 1012 | 1012 | 1012 | 1012 | 1012 | N/A | mA |
| | | XC7VX415T | 1324 | 1324 | 1324 | 1324 | 1324 | N/A | mA |
| | | XC7VX485T | 1578 | 1578 | 1578 | 1578 | 1578 | N/A | mA |
| | | XC7VX550T | 2214 | 2214 | 2214 | 2214 | 2214 | N/A | mA |
| | | XC7VX690T | 2214 | 2214 | 2214 | 2214 | 2214 | N/A | mA |
| | | XC7VX980T | N/A | 2580 | 2580 | 2580 | 2580 | N/A | mA |
| | | XC7VX1140T | N/A | 3448 | 3448 | 3448 | 3448 | N/A | mA |
| | | XQ7V585T | N/A | N/A | 1483 | 1483 | 1483 | 1483 | mA |
| | | XQ7VX330T | N/A | N/A | 1012 | 1012 | 1012 | 1012 | mA |
| | | XQ7VX485T | N/A | N/A | 1578 | 1578 | 1578 | 1578 | mA |
| | | XQ7VX690T | N/A | N/A | 2214 | N/A | 2214 | N/A | mA |
| XQ7VX980T | N/A | N/A | N/A | 2580 | 2580 | N/A | mA | | |

Table 6: Typical Quiescent Supply Current (Cont'd)

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---------------------|---|------------|-------------|-----|-----|-----|-----|-----|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| I _{CCOQ} | Quiescent V _{CCO} supply current | XC7V585T | 1 | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7V2000T | N/A | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7VX330T | 1 | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7VX415T | 1 | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7VX485T | 1 | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7VX550T | 1 | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7VX690T | 1 | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7VX980T | N/A | 1 | 1 | 1 | 1 | N/A | mA |
| | | XC7VX1140T | N/A | 1 | 1 | 1 | 1 | N/A | mA |
| | | XQ7V585T | N/A | N/A | 1 | 1 | 1 | 1 | mA |
| | | XQ7VX330T | N/A | N/A | 1 | 1 | 1 | 1 | mA |
| | | XQ7VX485T | N/A | N/A | 1 | 1 | 1 | 1 | mA |
| | | XQ7VX690T | N/A | N/A | 1 | N/A | 1 | N/A | mA |
| | | XQ7VX980T | N/A | N/A | N/A | 1 | 1 | N/A | mA |
| I _{CCAUXQ} | Quiescent V _{CCAUX} supply current | XC7V585T | 114 | 114 | 114 | 114 | 114 | N/A | mA |
| | | XC7V2000T | N/A | 315 | 315 | 315 | 315 | N/A | mA |
| | | XC7VX330T | 73 | 73 | 73 | 73 | 73 | N/A | mA |
| | | XC7VX415T | 88 | 88 | 88 | 88 | 88 | N/A | mA |
| | | XC7VX485T | 104 | 104 | 104 | 104 | 104 | N/A | mA |
| | | XC7VX550T | 147 | 147 | 147 | 147 | 147 | N/A | mA |
| | | XC7VX690T | 147 | 147 | 147 | 147 | 147 | N/A | mA |
| | | XC7VX980T | N/A | 183 | 183 | 183 | 183 | N/A | mA |
| | | XC7VX1140T | N/A | 250 | 250 | 250 | 250 | N/A | mA |
| | | XQ7V585T | N/A | N/A | 114 | 114 | 114 | 114 | mA |
| | | XQ7VX330T | N/A | N/A | 73 | 73 | 73 | 73 | mA |
| | | XQ7VX485T | N/A | N/A | 104 | 104 | 104 | 104 | mA |
| | | XQ7VX690T | N/A | N/A | 147 | N/A | 147 | N/A | mA |
| | | XQ7VX980T | N/A | N/A | N/A | 183 | 183 | N/A | mA |

Table 6: Typical Quiescent Supply Current (Cont'd)

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|------------------------|--|------------|-------------|-----|-----|-----|----|-----|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| I _{CCAUX_IOQ} | Quiescent V _{CCAUX_IO} supply current | XC7V585T | 2 | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7V2000T | N/A | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7VX330T | 2 | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7VX415T | 2 | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7VX485T | 2 | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7VX550T | 2 | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7VX690T | 2 | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7VX980T | N/A | 2 | 2 | 2 | 2 | N/A | mA |
| | | XC7VX1140T | N/A | 2 | 2 | 2 | 2 | N/A | mA |
| | | XQ7V585T | N/A | N/A | 2 | 2 | 2 | 2 | mA |
| | | XQ7VX330T | N/A | N/A | 2 | 2 | 2 | 2 | mA |
| | | XQ7VX485T | N/A | N/A | 2 | 2 | 2 | 2 | mA |
| | | XQ7VX690T | N/A | N/A | 2 | N/A | 2 | N/A | mA |
| | | XQ7VX980T | N/A | N/A | N/A | 2 | 2 | N/A | mA |
| I _{CCBRAMQ} | Quiescent V _{CCBRAM} supply current | XC7V585T | 34 | 34 | 34 | 34 | 34 | N/A | mA |
| | | XC7V2000T | N/A | 56 | 56 | 56 | 56 | N/A | mA |
| | | XC7VX330T | 32 | 32 | 32 | 32 | 32 | N/A | mA |
| | | XC7VX415T | 38 | 38 | 38 | 38 | 38 | N/A | mA |
| | | XC7VX485T | 44 | 44 | 44 | 44 | 44 | N/A | mA |
| | | XC7VX550T | 63 | 63 | 63 | 63 | 63 | N/A | mA |
| | | XC7VX690T | 63 | 63 | 63 | 63 | 63 | N/A | mA |
| | | XC7VX980T | N/A | 65 | 65 | 65 | 65 | N/A | mA |
| | | XC7VX1140T | N/A | 81 | 81 | 81 | 81 | N/A | mA |
| | | XQ7V585T | N/A | N/A | 34 | 34 | 34 | 34 | mA |
| | | XQ7VX330T | N/A | N/A | 32 | 32 | 32 | 32 | mA |
| | | XQ7VX485T | N/A | N/A | 44 | 44 | 44 | 44 | mA |
| | | XQ7VX690T | N/A | N/A | 63 | N/A | 63 | N/A | mA |
| | | XQ7VX980T | N/A | N/A | N/A | 65 | 65 | N/A | mA |

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

Table 7 shows the minimum current, in addition to I_{CCO} , that is required by Virtex-7 T and XT devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the Xilinx Power tools to estimate current drain on these supplies.

Table 7: Power-On Current for Virtex-7 T and XT Devices

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | I_{CCOMIN} | I_{CCAUX_IO} | I_{CCBRAM} | Units |
|------------|---------------------|--------------------|-----------------------------|----------------------------------|---------------------|-------|
| XC7V585T | $I_{CCINTQ} + 2700$ | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 60$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 108$ | mA |
| XC7V2000T | $I_{CCINTQ} + 4000$ | $I_{CCAUXQ} + 80$ | $I_{CCOQ} + 60$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 176$ | mA |
| XC7VX330T | $I_{CCINTQ} + 1000$ | $I_{CCAUXQ} + 65$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 95$ | mA |
| XC7VX415T | $I_{CCINTQ} + 1200$ | $I_{CCAUXQ} + 75$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 115$ | mA |
| XC7VX485T | $I_{CCINTQ} + 1200$ | $I_{CCAUXQ} + 80$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 140$ | mA |
| XC7VX550T | $I_{CCINTQ} + 3300$ | $I_{CCAUXQ} + 143$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 57$ mA per bank | $I_{CCBRAMQ} + 200$ | mA |
| XC7VX690T | $I_{CCINTQ} + 3300$ | $I_{CCAUXQ} + 143$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 57$ mA per bank | $I_{CCBRAMQ} + 200$ | mA |
| XC7VX980T | $I_{CCINTQ} + 6500$ | $I_{CCAUXQ} + 202$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 60$ mA per bank | $I_{CCBRAMQ} + 204$ | mA |
| XC7VX1140T | $I_{CCINTQ} + 8000$ | $I_{CCAUXQ} + 235$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 63$ mA per bank | $I_{CCBRAMQ} + 256$ | mA |
| XQ7V585T | $I_{CCINTQ} + 2700$ | $I_{CCAUXQ} + 40$ | $I_{CCOQ} + 60$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 108$ | mA |
| XQ7VX330T | $I_{CCINTQ} + 1000$ | $I_{CCAUXQ} + 65$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 95$ | mA |
| XQ7VX485T | $I_{CCINTQ} + 1200$ | $I_{CCAUXQ} + 80$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 40$ mA per bank | $I_{CCBRAMQ} + 140$ | mA |
| XQ7VX690T | $I_{CCINTQ} + 3300$ | $I_{CCAUXQ} + 143$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 57$ mA per bank | $I_{CCBRAMQ} + 200$ | mA |
| XQ7VX980T | $I_{CCINTQ} + 6500$ | $I_{CCAUXQ} + 202$ | $I_{CCOQ} + 40$ mA per bank | $I_{CCOAUxIOQ} + 60$ mA per bank | $I_{CCBRAMQ} + 204$ | mA |

Table 8: Power Supply Ramp Time

| Symbol | Description | Conditions | Min | Max | Units |
|-------------------|---|----------------------------|-----|-----|-------|
| T_{VCCINT} | Ramp time from GND to 90% of V_{CCINT} | | 0.2 | 50 | ms |
| T_{VCCO} | Ramp time from GND to 90% of V_{CCO} | | 0.2 | 50 | ms |
| T_{VCCAUX} | Ramp time from GND to 90% of V_{CCAUX} | | 0.2 | 50 | ms |
| T_{VCCAUX_IO} | Ramp time from GND to 90% of V_{CCAUX_IO} | | 0.2 | 50 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 90% of V_{CCBRAM} | | 0.2 | 50 | ms |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ | $T_J = 125^{\circ}C^{(1)}$ | – | 300 | ms |
| | | $T_J = 100^{\circ}C^{(1)}$ | – | 500 | |
| | | $T_J = 85^{\circ}C^{(1)}$ | – | 800 | |
| $T_{MGTAVCC}$ | Ramp time from GND to 90% of $V_{MGTAVCC}$ | | 0.2 | 50 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 90% of $V_{MGTAVTT}$ | | 0.2 | 50 | ms |
| $T_{MGTVCCAUX}$ | Ramp time from GND to 90% of $V_{MGTVCCAUX}$ | | 0.2 | 50 | ms |

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾

| I/O Standard | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} |
|------------------------|----------|-------------------|-------------------|-------------------|---------------------|---------------------|----------|----------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | 8 | -8 |
| HSTL_I_12 | -0.300 | $V_{REF} - 0.080$ | $V_{REF} + 0.080$ | $V_{CCO} + 0.300$ | 25% V_{CCO} | 75% V_{CCO} | 6.3 | -6.3 |
| HSTL_I_18 | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | 8 | -8 |
| HSTL_II | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | 16 | -16 |
| HSTL_II_18 | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | 16 | -16 |
| HSUL_12 | -0.300 | $V_{REF} - 0.130$ | $V_{REF} + 0.130$ | $V_{CCO} + 0.300$ | 20% V_{CCO} | 80% V_{CCO} | 0.1 | -0.1 |
| LVC MOS12 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | Note 3 | Note 3 |
| LVC MOS15, LVDCI_15 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 25% V_{CCO} | 75% V_{CCO} | Note 4 | Note 4 |
| LVC MOS18, LVDCI_18 | -0.300 | 35% V_{CCO} | 65% V_{CCO} | $V_{CCO} + 0.300$ | 0.450 | $V_{CCO} - 0.450$ | Note 5 | Note 5 |
| LVC MOS25 | -0.300 | 0.700 | 1.700 | $V_{CCO} + 0.300$ | 0.400 | $V_{CCO} - 0.400$ | Note 6 | Note 6 |
| LVC MOS33 | -0.300 | 0.800 | 2.000 | 3.450 | 0.400 | $V_{CCO} - 0.400$ | Note 6 | Note 6 |
| LV TTL | -0.300 | 0.800 | 2.000 | 3.450 | 0.400 | 2.400 | Note 7 | Note 7 |
| MOBILE_DDR | -0.300 | 20% V_{CCO} | 80% V_{CCO} | $V_{CCO} + 0.300$ | 10% V_{CCO} | 90% V_{CCO} | 0.1 | -0.1 |
| PCI33_3 | -0.400 | 30% V_{CCO} | 50% V_{CCO} | $V_{CCO} + 0.500$ | 10% V_{CCO} | 90% V_{CCO} | 1.5 | -0.5 |
| SSTL12 | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 14.25 | -14.25 |
| SSTL135 | -0.300 | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 13.0 | -13.0 |
| SSTL135_R | -0.300 | $V_{REF} - 0.090$ | $V_{REF} + 0.090$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.150$ | $V_{CCO}/2 + 0.150$ | 8.9 | -8.9 |
| SSTL15 | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 13.0 | -13.0 |
| SSTL15_R | -0.300 | $V_{REF} - 0.100$ | $V_{REF} + 0.100$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.175$ | $V_{CCO}/2 + 0.175$ | 8.9 | -8.9 |
| SSTL18_I | -0.300 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.470$ | $V_{CCO}/2 + 0.470$ | 8 | -8 |
| SSTL18_II | -0.300 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCO} + 0.300$ | $V_{CCO}/2 - 0.600$ | $V_{CCO}/2 + 0.600$ | 13.4 | -13.4 |

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)).

Table 10: Differential SelectIO DC Input and Output Levels

| I/O Standard | $V_{ICM}^{(1)}$ | | | $V_{ID}^{(2)}$ | | | $V_{OCM}^{(3)}$ | | | $V_{OD}^{(4)}$ | | |
|--------------|-----------------|--------|-------------|----------------|--------|--------|-----------------|-----------------|-----------------|----------------|--------|--------|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | V_{CCAUX} | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | V_{CCAUX} | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}-0.405$ | $V_{CCO}-0.300$ | $V_{CCO}-0.190$ | 0.400 | 0.600 | 0.800 |

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \bar{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage ($Q - \bar{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 12.
7. LVDS is specified in Table 13.

Table 11: Complementary Differential SelectIO DC Input and Output Levels

| I/O Standard | $V_{ICM}^{(1)}$ | | | $V_{ID}^{(2)}$ | | $V_{OL}^{(3)}$ | $V_{OH}^{(4)}$ | I_{OL} | I_{OH} |
|-----------------|-----------------|--------|--------|----------------|--------|-----------------------|-----------------------|----------|----------|
| | V, Min | V, Typ | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}-0.400$ | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}-0.400$ | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}-0.400$ | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}-0.400$ | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% V_{CCO} | 80% V_{CCO} | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% V_{CCO} | 90% V_{CCO} | 0.100 | –0.100 |
| DIFF_SSTL12 | 0.300 | 0.600 | 0.850 | 0.100 | – | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 14.25 | –14.25 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | $(V_{CCO}/2) - 0.470$ | $(V_{CCO}/2) + 0.470$ | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | $(V_{CCO}/2) - 0.600$ | $(V_{CCO}/2) + 0.600$ | 13.4 | –13.4 |

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \bar{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: LVDS_25 DC Specifications⁽¹⁾

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|--------------------|---|---|-------|-------|-------|-------|
| V _{CCO} | Supply voltage | | 2.375 | 2.500 | 2.625 | V |
| V _{OH} | Output High voltage for Q and \bar{Q} | R _T = 100 Ω across Q and \bar{Q} signals | – | – | 1.675 | V |
| V _{OL} | Output Low voltage for Q and \bar{Q} | R _T = 100 Ω across Q and \bar{Q} signals | 0.700 | – | – | V |
| V _{ODIFF} | Differential output voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High | R _T = 100 Ω across Q and \bar{Q} signals | 247 | 350 | 600 | mV |
| V _{OCM} | Output common-mode voltage | R _T = 100 Ω across Q and \bar{Q} signals | 1.000 | 1.250 | 1.425 | V |
| V _{IDIFF} | Differential input voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High | | 100 | 350 | 600 | mV |
| V _{ICM} | Input common-mode voltage | | 0.300 | 1.200 | 1.500 | V |

Notes:

- Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide (UG471)* for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: LVDS DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|--------------------|---|---|-------|-------|-------|-------|
| V _{CCO} | Supply voltage | | 1.710 | 1.800 | 1.890 | V |
| V _{OH} | Output High voltage for Q and \bar{Q} | R _T = 100 Ω across Q and \bar{Q} signals | – | – | 1.675 | V |
| V _{OL} | Output Low voltage for Q and \bar{Q} | R _T = 100 Ω across Q and \bar{Q} signals | 0.825 | – | – | V |
| V _{ODIFF} | Differential output voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High | R _T = 100 Ω across Q and \bar{Q} signals | 247 | 350 | 600 | mV |
| V _{OCM} | Output common-mode voltage | R _T = 100 Ω across Q and \bar{Q} signals | 1.000 | 1.250 | 1.425 | V |
| V _{IDIFF} | Differential input voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High | Common-mode input voltage = 1.25V | 100 | 350 | 600 | mV |
| V _{ICM} | Input common-mode voltage | Differential input voltage = ±350 mV | 0.300 | 1.200 | 1.425 | V |

Notes:

- Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide (UG471)* for more information.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.7 and Vivado® Design Suite 2013.4 as outlined in [Table 14](#).

Table 14: Virtex-7 T and XT FPGA Speed Specification Version By Device

| Version In: | | Typical V _{CCINT} (Table 2) | Device |
|-------------|---------------|---|---|
| ISE 14.7 | Vivado 2013.4 | | |
| 1.05 | 1.06 | 1.0V | XQ7V585T, XQ7VX485T |
| 1.06 | 1.07 | 1.0V | XQ7VX330T, XQ7VX690T, XQ7VX980T |
| 1.10 | 1.11 | 1.0V | XC7V585T, XC7VX485T |
| N/A | 1.10 | 1.0V | XC7V2000T |
| 1.10 | 1.11 | 1.0V | XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T |
| N/A | 1.11 | 1.0V | XC7VX1140T |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-7 T and XT FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 15](#) correlates the current status of each Virtex-7 T and XT device on a per speed grade basis.

Table 15: Virtex-7 T and XT Device Speed Grade Designations

| Device | Speed Grade Designations | | |
|------------|--------------------------|-------------|--------------------|
| | Advance | Preliminary | Production |
| XC7V585T | | | -3, -2, -2L, -1 |
| XC7V2000T | | | -2, -2L, -2G, -1 |
| XC7VX330T | | | -3, -2, -2L, -1 |
| XC7VX415T | | | -3, -2, -2L, -1 |
| XC7VX485T | | | -3, -2, -2L, -1 |
| XC7VX550T | | | -3, -2, -2L, -1 |
| XC7VX690T | | | -3, -2, -2L, -1 |
| XC7VX980T | | | -2, -2L, -1 |
| XC7VX1140T | | | -2, -2L, -2G, -1 |
| XQ7V585T | | | -2, -2L, -1I, -1M |
| XQ7VX330T | | | -2, -2L, -1I, -1M |
| XQ7VX485T | | | -2I, -2L, -1I, -1M |
| XQ7VX690T | | | -2I, -1I |
| XQ7VX980T | | | -2L, -1I |

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 16](#) lists the production released Virtex-7 T and XT device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: Virtex-7 T and XT Device Production Software and Speed Specification Release

| Device | Speed Grade Designations | | | | | |
|-----------|--|---------------------------|---|-----|----|-----|
| | -3 | -2G | -2 | -2L | -1 | -1M |
| XC7V585T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 | N/A | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 | | | N/A |
| XC7V2000T | N/A | Vivado tools 2012.4 v1.07 | | | | N/A |
| XC7VX330T | Vivado tools 2013.1 v1.08 or ISE tools 14.5 v1.08 | N/A | Vivado tools 2013.1 v1.08 or ISE tools 14.5 v1.08 | | | N/A |
| XC7VX415T | | N/A | | | | N/A |
| XC7VX485T | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 | N/A | Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06 | | | N/A |
| XC7VX550T | Vivado tools 2013.1 v1.08 or ISE tools 14.5 v1.08 | N/A | Vivado tools 2013.1 v1.08 or ISE tools 14.5 v1.08 | | | N/A |
| XC7VX690T | Vivado tools 2013.1 v1.08 or ISE tools 14.5 v1.08 | N/A | Vivado tools 2013.1 v1.08 or ISE tools 14.5 v1.08 | | | N/A |
| XC7VX980T | N/A | N/A | Vivado tools 2013.1 v1.08 or ISE tools 14.5 v1.08 | | | N/A |

Table 16: Virtex-7 T and XT Device Production Software and Speed Specification Release (Cont'd)

| Device | Speed Grade Designations | | | | | |
|------------|--------------------------|---------------------------|---|---|---|---|
| | -3 | -2G | -2 | -2L | -1 | -1M |
| XC7VX1140T | N/A | Vivado tools 2013.1 v1.08 | | | | N/A |
| XQ7V585T | N/A | N/A | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 | | | |
| XQ7VX330T | N/A | N/A | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 | | | Vivado tools 2013.2 v1.05 or ISE tools 14.6 v1.05 |
| XQ7VX485T | N/A | N/A | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 | | | |
| XQ7VX690T | N/A | N/A | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 | N/A | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 | N/A |
| XQ7VX980T | N/A | N/A | N/A | Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04 | | N/A |

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 T and XT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 13](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: Networking Applications Interface Performances

| Description | I/O Bank Type | Speed Grade | | | Units |
|--|---------------|-------------|------------|--------|-------|
| | | -3 | -2/-2L/-2G | -1/-1M | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | HR | 710 | 710 | 625 | Mb/s |
| | HP | 710 | 710 | 625 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | HR | 1250 | 1250 | 950 | Mb/s |
| | HP | 1600 | 1400 | 1250 | Mb/s |
| SDR LVDS receiver (SFI-4.1) ⁽¹⁾ | HR | 710 | 710 | 625 | Mb/s |
| | HP | 710 | 710 | 625 | Mb/s |
| DDR LVDS receiver (SPI-4.2) ⁽¹⁾ | HR | 1250 | 1250 | 950 | Mb/s |
| | HP | 1600 | 1400 | 1250 | Mb/s |

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

[Table 18](#) provides the maximum data rates for applicable memory standards using the Virtex-7 T and XT FPGAs memory PHY. The final performance of the memory interface is determined through a complete design implemented in the Vivado or ISE Design Suite, following guidelines in the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide (UG586)*, electrical analysis, and characterization of the system.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator⁽¹⁾⁽²⁾

| Memory Standard | I/O Bank Type | V _{CCAUX_IO} | Speed Grade | | | | Units |
|-------------------------------|---------------|-----------------------|---------------------|---------------------|------|------|-------|
| | | | -3 | -2/-2L/-2G | -1 | -1M | |
| 4:1 Memory Controllers | | | | | | | |
| DDR3 | HP | 2.0V | 1866 ⁽³⁾ | 1866 ⁽³⁾ | 1600 | 1066 | Mb/s |
| | HP | 1.8V | 1600 | 1333 | 1066 | 800 | |
| | HR | N/A | 1066 | 1066 | 800 | 800 | |
| DDR3L | HP | 2.0V | 1600 | 1600 | 1333 | 1066 | Mb/s |
| | HP | 1.8V | 1333 | 1066 | 800 | 800 | |
| | HR | N/A | 800 | 800 | 667 | N/A | |
| DDR2 | HP | 2.0V | 800 | 800 | 800 | 667 | Mb/s |
| | HP | 1.8V | | | | 533 | |
| | HR | N/A | | | | 533 | |
| RLDRAM III | HP | 2.0V | 800 | 667 | 667 | 550 | MHz |
| | HP | 1.8V | 550 | 500 | 450 | 400 | |
| | HR | N/A | N/A | | | | |
| 2:1 Memory Controllers | | | | | | | |
| DDR3 | HP | 2.0V | 1066 | 1066 | 800 | 667 | Mb/s |
| | HP | 1.8V | | | | 667 | |
| | HR | N/A | | | | 667 | |
| DDR3L | HP | 2.0V | 1066 | 1066 | 800 | 667 | Mb/s |
| | HP | 1.8V | | | | 667 | |
| | HR | N/A | | | | N/A | |
| DDR2 | HP | 2.0V | 800 | 800 | 800 | 667 | Mb/s |
| | HP | 1.8V | | | | 533 | |
| | HR | N/A | | | | 533 | |
| QDR II+ ⁽⁴⁾ | HP | 2.0V | 550 | 500 | 450 | 300 | MHz |
| | HP | 1.8V | | | | 300 | |
| | HR | N/A | | | | 300 | |
| RLDRAM II | HP | 2.0V | 533 | 500 | 450 | 400 | MHz |
| | HP | 1.8V | | | | 400 | |
| | HR | N/A | | | | 400 | |
| LPDDR2 | HP | 2.0V | 667 | 667 | 667 | 533 | Mb/s |
| | HP | 1.8V | | | | 533 | |
| | HR | N/A | | | | 533 | |

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions User Guide (UG586)*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. For designs using 1866 Mb/s components, contact [Xilinx Technical Support](#).
4. The maximum QDR II+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

| I/O Standard | T_{IOPI} | | | | T_{IOOP} | | | | T_{IOTP} | | | | Units |
|--------------------------|-------------|------------|------|------|-------------|------------|------|------|-------------|------------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | |
| LVTTTL_S4 | 1.31 | 1.42 | 1.64 | 1.64 | 3.77 | 3.90 | 4.00 | 4.00 | 3.52 | 3.67 | 3.86 | 3.86 | ns |
| LVTTTL_S8 | 1.31 | 1.42 | 1.64 | 1.64 | 3.50 | 3.64 | 3.73 | 3.73 | 3.26 | 3.40 | 3.60 | 3.60 | ns |
| LVTTTL_S12 | 1.31 | 1.42 | 1.64 | 1.64 | 3.49 | 3.62 | 3.72 | 3.72 | 3.24 | 3.39 | 3.58 | 3.58 | ns |
| LVTTTL_S16 | 1.31 | 1.42 | 1.64 | 1.64 | 3.03 | 3.17 | 3.26 | 3.26 | 2.79 | 2.93 | 3.13 | 3.13 | ns |
| LVTTTL_S24 | 1.31 | 1.42 | 1.64 | 1.64 | 3.25 | 3.39 | 3.48 | 3.48 | 3.01 | 3.15 | 3.35 | 3.35 | ns |
| LVTTTL_F4 | 1.31 | 1.42 | 1.64 | 1.64 | 3.22 | 3.36 | 3.45 | 3.45 | 2.98 | 3.12 | 3.32 | 3.32 | ns |
| LVTTTL_F8 | 1.31 | 1.42 | 1.64 | 1.64 | 2.71 | 2.84 | 2.93 | 2.93 | 2.46 | 2.61 | 2.80 | 2.80 | ns |
| LVTTTL_F12 | 1.31 | 1.42 | 1.64 | 1.64 | 2.69 | 2.82 | 2.92 | 2.92 | 2.44 | 2.59 | 2.79 | 2.79 | ns |
| LVTTTL_F16 | 1.31 | 1.42 | 1.64 | 1.64 | 2.57 | 2.85 | 3.15 | 3.15 | 2.33 | 2.61 | 3.02 | 3.02 | ns |
| LVTTTL_F24 | 1.31 | 1.42 | 1.64 | 1.64 | 2.41 | 2.64 | 2.89 | 3.04 | 2.16 | 2.41 | 2.76 | 2.91 | ns |
| LVDS_25 | 0.64 | 0.68 | 0.80 | 0.87 | 1.36 | 1.47 | 1.55 | 1.55 | 1.11 | 1.24 | 1.41 | 1.41 | ns |
| MINI_LVDS_25 | 0.68 | 0.70 | 0.79 | 0.87 | 1.36 | 1.47 | 1.55 | 1.55 | 1.11 | 1.24 | 1.41 | 1.41 | ns |
| BLVDS_25 | 0.65 | 0.69 | 0.80 | 0.85 | 1.83 | 2.02 | 2.20 | 2.57 | 1.59 | 1.79 | 2.07 | 2.44 | ns |
| RSDS_25 (point to point) | 0.63 | 0.68 | 0.79 | 0.87 | 1.36 | 1.48 | 1.55 | 1.55 | 1.11 | 1.24 | 1.41 | 1.41 | ns |
| PPDS_25 | 0.65 | 0.69 | 0.80 | 0.87 | 1.36 | 1.49 | 1.58 | 1.58 | 1.11 | 1.25 | 1.45 | 1.45 | ns |
| TMDS_33 | 0.72 | 0.76 | 0.86 | 0.90 | 1.43 | 1.54 | 1.60 | 1.60 | 1.18 | 1.31 | 1.47 | 1.47 | ns |
| PCI33_3 | 1.28 | 1.41 | 1.65 | 1.65 | 2.71 | 3.08 | 3.52 | 3.52 | 2.46 | 2.84 | 3.39 | 3.39 | ns |
| HSUL_12_S | 0.63 | 0.64 | 0.71 | 0.85 | 1.77 | 1.90 | 2.00 | 2.00 | 1.52 | 1.67 | 1.86 | 1.86 | ns |
| HSUL_12_F | 0.63 | 0.64 | 0.71 | 0.85 | 1.26 | 1.40 | 1.50 | 1.50 | 1.01 | 1.16 | 1.37 | 1.37 | ns |
| DIFF_HSUL_12_S | 0.58 | 0.61 | 0.70 | 0.84 | 1.55 | 1.68 | 1.78 | 1.78 | 1.30 | 1.45 | 1.65 | 1.65 | ns |
| DIFF_HSUL_12_F | 0.58 | 0.61 | 0.70 | 0.84 | 1.16 | 1.28 | 1.35 | 1.35 | 0.92 | 1.04 | 1.21 | 1.21 | ns |
| MOBILE_DDR_S | 0.64 | 0.66 | 0.74 | 0.74 | 2.58 | 2.91 | 3.31 | 3.31 | 2.33 | 2.68 | 3.17 | 3.17 | ns |
| MOBILE_DDR_F | 0.64 | 0.66 | 0.74 | 0.74 | 1.91 | 2.13 | 2.36 | 2.36 | 1.66 | 1.89 | 2.23 | 2.23 | ns |
| DIFF_MOBILE_DDR_S | 0.63 | 0.66 | 0.75 | 0.75 | 2.51 | 2.84 | 3.24 | 3.24 | 2.26 | 2.61 | 3.10 | 3.10 | ns |
| DIFF_MOBILE_DDR_F | 0.63 | 0.66 | 0.75 | 0.75 | 1.89 | 2.11 | 2.34 | 2.34 | 1.64 | 1.88 | 2.21 | 2.21 | ns |
| HSTL_I_S | 0.61 | 0.64 | 0.73 | 0.84 | 1.55 | 1.69 | 1.80 | 1.80 | 1.30 | 1.46 | 1.67 | 1.67 | ns |
| HSTL_II_S | 0.61 | 0.64 | 0.73 | 0.84 | 1.21 | 1.34 | 1.43 | 1.61 | 0.96 | 1.11 | 1.30 | 1.47 | ns |
| HSTL_I_18_S | 0.64 | 0.67 | 0.76 | 0.85 | 1.28 | 1.39 | 1.45 | 1.45 | 1.04 | 1.16 | 1.31 | 1.32 | ns |
| HSTL_II_18_S | 0.64 | 0.67 | 0.76 | 0.85 | 1.18 | 1.31 | 1.40 | 1.57 | 0.93 | 1.08 | 1.27 | 1.44 | ns |

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|-------------------|-------------------|------------|------|------|-------------------|------------|------|------|-------------------|------------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | |
| DIFF_HSTL_I_S | 0.63 | 0.67 | 0.77 | 0.84 | 1.42 | 1.54 | 1.61 | 1.78 | 1.17 | 1.31 | 1.48 | 1.65 | ns |
| DIFF_HSTL_II_S | 0.63 | 0.67 | 0.77 | 0.84 | 1.15 | 1.24 | 1.27 | 1.61 | 0.91 | 1.01 | 1.14 | 1.47 | ns |
| DIFF_HSTL_I_18_S | 0.65 | 0.69 | 0.78 | 0.84 | 1.27 | 1.38 | 1.43 | 1.45 | 1.03 | 1.14 | 1.30 | 1.32 | ns |
| DIFF_HSTL_II_18_S | 0.65 | 0.69 | 0.78 | 0.85 | 1.14 | 1.23 | 1.26 | 1.57 | 0.90 | 1.00 | 1.13 | 1.44 | ns |
| HSTL_I_F | 0.61 | 0.64 | 0.73 | 0.84 | 1.10 | 1.19 | 1.23 | 1.31 | 0.85 | 0.96 | 1.10 | 1.18 | ns |
| HSTL_II_F | 0.61 | 0.64 | 0.73 | 0.84 | 1.05 | 1.18 | 1.28 | 1.31 | 0.80 | 0.95 | 1.15 | 1.18 | ns |
| HSTL_I_18_F | 0.64 | 0.67 | 0.76 | 0.85 | 1.05 | 1.18 | 1.28 | 1.36 | 0.80 | 0.95 | 1.15 | 1.22 | ns |
| HSTL_II_18_F | 0.64 | 0.67 | 0.76 | 0.85 | 1.03 | 1.14 | 1.23 | 1.32 | 0.78 | 0.90 | 1.10 | 1.19 | ns |
| DIFF_HSTL_I_F | 0.63 | 0.67 | 0.77 | 0.84 | 1.09 | 1.18 | 1.22 | 1.31 | 0.84 | 0.95 | 1.09 | 1.18 | ns |
| DIFF_HSTL_II_F | 0.63 | 0.67 | 0.77 | 0.84 | 1.02 | 1.11 | 1.14 | 1.31 | 0.77 | 0.88 | 1.01 | 1.18 | ns |
| DIFF_HSTL_I_18_F | 0.65 | 0.69 | 0.78 | 0.84 | 1.08 | 1.17 | 1.21 | 1.36 | 0.83 | 0.94 | 1.07 | 1.22 | ns |
| DIFF_HSTL_II_18_F | 0.65 | 0.69 | 0.78 | 0.85 | 1.01 | 1.10 | 1.13 | 1.32 | 0.76 | 0.87 | 1.00 | 1.19 | ns |
| LVC MOS33_S4 | 1.31 | 1.40 | 1.60 | 1.60 | 3.77 | 3.90 | 4.00 | 4.00 | 3.52 | 3.67 | 3.86 | 3.86 | ns |
| LVC MOS33_S8 | 1.31 | 1.40 | 1.60 | 1.60 | 3.49 | 3.62 | 3.72 | 3.72 | 3.24 | 3.39 | 3.58 | 3.58 | ns |
| LVC MOS33_S12 | 1.31 | 1.40 | 1.60 | 1.60 | 3.05 | 3.18 | 3.28 | 3.28 | 2.80 | 2.95 | 3.15 | 3.15 | ns |
| LVC MOS33_S16 | 1.31 | 1.40 | 1.60 | 1.60 | 3.06 | 3.43 | 3.88 | 3.88 | 2.81 | 3.20 | 3.75 | 3.75 | ns |
| LVC MOS33_F4 | 1.31 | 1.40 | 1.60 | 1.60 | 3.22 | 3.36 | 3.45 | 3.45 | 2.98 | 3.12 | 3.32 | 3.32 | ns |
| LVC MOS33_F8 | 1.31 | 1.40 | 1.60 | 1.60 | 2.71 | 2.84 | 2.93 | 2.93 | 2.46 | 2.61 | 2.80 | 2.80 | ns |
| LVC MOS33_F12 | 1.31 | 1.40 | 1.60 | 1.60 | 2.57 | 2.85 | 3.15 | 3.15 | 2.33 | 2.61 | 3.02 | 3.02 | ns |
| LVC MOS33_F16 | 1.31 | 1.40 | 1.60 | 1.60 | 2.44 | 2.69 | 2.96 | 2.96 | 2.19 | 2.45 | 2.82 | 2.82 | ns |
| LVC MOS25_S4 | 1.08 | 1.16 | 1.32 | 1.35 | 3.08 | 3.22 | 3.31 | 3.31 | 2.84 | 2.98 | 3.18 | 3.18 | ns |
| LVC MOS25_S8 | 1.08 | 1.16 | 1.32 | 1.35 | 2.85 | 2.98 | 3.07 | 3.08 | 2.60 | 2.75 | 2.94 | 2.94 | ns |
| LVC MOS25_S12 | 1.08 | 1.16 | 1.32 | 1.35 | 2.44 | 2.57 | 2.67 | 2.67 | 2.19 | 2.34 | 2.54 | 2.54 | ns |
| LVC MOS25_S16 | 1.08 | 1.16 | 1.32 | 1.35 | 2.79 | 2.92 | 3.01 | 3.01 | 2.54 | 2.68 | 2.88 | 2.88 | ns |
| LVC MOS25_F4 | 1.08 | 1.16 | 1.32 | 1.35 | 2.71 | 2.84 | 2.93 | 2.93 | 2.46 | 2.61 | 2.80 | 2.80 | ns |
| LVC MOS25_F8 | 1.08 | 1.16 | 1.32 | 1.35 | 2.14 | 2.28 | 2.37 | 2.37 | 1.90 | 2.04 | 2.24 | 2.24 | ns |
| LVC MOS25_F12 | 1.08 | 1.16 | 1.32 | 1.35 | 2.15 | 2.29 | 2.52 | 2.52 | 1.91 | 2.05 | 2.38 | 2.38 | ns |
| LVC MOS25_F16 | 1.08 | 1.16 | 1.32 | 1.35 | 1.92 | 2.17 | 2.45 | 2.45 | 1.67 | 1.94 | 2.32 | 2.32 | ns |
| LVC MOS18_S4 | 0.64 | 0.66 | 0.74 | 0.95 | 1.55 | 1.68 | 1.78 | 1.78 | 1.30 | 1.45 | 1.65 | 1.65 | ns |
| LVC MOS18_S8 | 0.64 | 0.66 | 0.74 | 0.95 | 2.14 | 2.28 | 2.37 | 2.37 | 1.90 | 2.04 | 2.24 | 2.24 | ns |
| LVC MOS18_S12 | 0.64 | 0.66 | 0.74 | 0.95 | 2.14 | 2.28 | 2.37 | 2.37 | 1.90 | 2.04 | 2.24 | 2.24 | ns |
| LVC MOS18_S16 | 0.64 | 0.66 | 0.74 | 0.95 | 1.49 | 1.62 | 1.72 | 1.72 | 1.24 | 1.39 | 1.58 | 1.58 | ns |
| LVC MOS18_S24 | 0.64 | 0.66 | 0.74 | 0.95 | 1.74 | 1.92 | 2.08 | 2.22 | 1.50 | 1.69 | 1.95 | 2.08 | ns |
| LVC MOS18_F4 | 0.64 | 0.66 | 0.74 | 0.95 | 1.38 | 1.51 | 1.61 | 1.64 | 1.13 | 1.28 | 1.47 | 1.50 | ns |
| LVC MOS18_F8 | 0.64 | 0.66 | 0.74 | 0.95 | 1.64 | 1.78 | 1.87 | 1.87 | 1.40 | 1.54 | 1.74 | 1.74 | ns |
| LVC MOS18_F12 | 0.64 | 0.66 | 0.74 | 0.95 | 1.64 | 1.78 | 1.87 | 1.87 | 1.40 | 1.54 | 1.74 | 1.74 | ns |
| LVC MOS18_F16 | 0.64 | 0.66 | 0.74 | 0.95 | 1.52 | 1.68 | 1.81 | 1.81 | 1.28 | 1.45 | 1.68 | 1.68 | ns |
| LVC MOS18_F24 | 0.64 | 0.66 | 0.74 | 0.95 | 1.34 | 1.46 | 1.55 | 2.09 | 1.09 | 1.23 | 1.42 | 1.96 | ns |
| LVC MOS15_S4 | 0.66 | 0.69 | 0.81 | 0.93 | 1.86 | 2.00 | 2.09 | 2.09 | 1.62 | 1.76 | 1.96 | 1.96 | ns |
| LVC MOS15_S8 | 0.66 | 0.69 | 0.81 | 0.93 | 2.05 | 2.18 | 2.28 | 2.28 | 1.80 | 1.95 | 2.14 | 2.15 | ns |

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|------------------|-------------------|------------|------|------|-------------------|------------|------|------|-------------------|------------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | |
| LVC MOS15_S12 | 0.66 | 0.69 | 0.81 | 0.93 | 1.83 | 2.03 | 2.23 | 2.23 | 1.59 | 1.80 | 2.10 | 2.10 | ns |
| LVC MOS15_S16 | 0.66 | 0.69 | 0.81 | 0.93 | 1.76 | 1.95 | 2.13 | 2.13 | 1.52 | 1.72 | 1.99 | 1.99 | ns |
| LVC MOS15_F4 | 0.66 | 0.69 | 0.81 | 0.93 | 1.63 | 1.76 | 1.86 | 1.86 | 1.38 | 1.53 | 1.72 | 1.72 | ns |
| LVC MOS15_F8 | 0.66 | 0.69 | 0.81 | 0.93 | 1.79 | 1.99 | 2.18 | 2.18 | 1.55 | 1.76 | 2.05 | 2.05 | ns |
| LVC MOS15_F12 | 0.66 | 0.69 | 0.81 | 0.93 | 1.40 | 1.54 | 1.65 | 1.65 | 1.15 | 1.31 | 1.52 | 1.52 | ns |
| LVC MOS15_F16 | 0.66 | 0.69 | 0.81 | 0.93 | 1.37 | 1.51 | 1.61 | 1.89 | 1.13 | 1.27 | 1.48 | 1.75 | ns |
| LVC MOS12_S4 | 0.88 | 0.91 | 1.00 | 1.17 | 2.53 | 2.67 | 2.76 | 2.76 | 2.29 | 2.43 | 2.63 | 2.63 | ns |
| LVC MOS12_S8 | 0.88 | 0.91 | 1.00 | 1.17 | 2.05 | 2.18 | 2.28 | 2.28 | 1.80 | 1.95 | 2.14 | 2.15 | ns |
| LVC MOS12_S12 | 0.88 | 0.91 | 1.00 | 1.17 | 1.75 | 1.89 | 1.98 | 1.98 | 1.51 | 1.65 | 1.85 | 1.85 | ns |
| LVC MOS12_F4 | 0.88 | 0.91 | 1.00 | 1.17 | 1.94 | 2.07 | 2.17 | 2.17 | 1.69 | 1.84 | 2.04 | 2.04 | ns |
| LVC MOS12_F8 | 0.88 | 0.91 | 1.00 | 1.17 | 1.50 | 1.64 | 1.73 | 1.73 | 1.26 | 1.40 | 1.60 | 1.60 | ns |
| LVC MOS12_F12 | 0.88 | 0.91 | 1.00 | 1.17 | 1.54 | 1.71 | 1.87 | 1.87 | 1.29 | 1.48 | 1.74 | 1.74 | ns |
| SSTL135_S | 0.61 | 0.64 | 0.73 | 0.85 | 1.27 | 1.40 | 1.50 | 1.53 | 1.02 | 1.17 | 1.36 | 1.40 | ns |
| SSTL15_S | 0.61 | 0.64 | 0.73 | 0.73 | 1.24 | 1.37 | 1.47 | 1.53 | 0.99 | 1.14 | 1.33 | 1.40 | ns |
| SSTL18_I_S | 0.64 | 0.67 | 0.76 | 0.84 | 1.59 | 1.74 | 1.85 | 1.85 | 1.34 | 1.50 | 1.72 | 1.72 | ns |
| SSTL18_II_S | 0.64 | 0.67 | 0.76 | 0.85 | 1.27 | 1.40 | 1.50 | 1.50 | 1.02 | 1.17 | 1.36 | 1.36 | ns |
| DIFF_SSTL135_S | 0.59 | 0.61 | 0.73 | 0.85 | 1.27 | 1.40 | 1.50 | 1.53 | 1.02 | 1.17 | 1.36 | 1.40 | ns |
| DIFF_SSTL15_S | 0.63 | 0.67 | 0.77 | 0.85 | 1.24 | 1.37 | 1.47 | 1.53 | 0.99 | 1.14 | 1.33 | 1.40 | ns |
| DIFF_SSTL18_I_S | 0.65 | 0.69 | 0.78 | 0.85 | 1.50 | 1.63 | 1.72 | 1.82 | 1.26 | 1.40 | 1.59 | 1.69 | ns |
| DIFF_SSTL18_II_S | 0.65 | 0.69 | 0.78 | 0.85 | 1.13 | 1.22 | 1.25 | 1.50 | 0.88 | 0.99 | 1.12 | 1.36 | ns |
| SSTL135_F | 0.61 | 0.64 | 0.73 | 0.85 | 1.04 | 1.17 | 1.26 | 1.31 | 0.79 | 0.93 | 1.13 | 1.18 | ns |
| SSTL15_F | 0.61 | 0.64 | 0.73 | 0.73 | 1.04 | 1.17 | 1.26 | 1.26 | 0.79 | 0.93 | 1.13 | 1.13 | ns |
| SSTL18_I_F | 0.64 | 0.67 | 0.76 | 0.84 | 1.12 | 1.22 | 1.26 | 1.34 | 0.88 | 0.99 | 1.13 | 1.21 | ns |
| SSTL18_II_F | 0.64 | 0.67 | 0.76 | 0.85 | 1.05 | 1.18 | 1.28 | 1.32 | 0.80 | 0.95 | 1.15 | 1.19 | ns |
| DIFF_SSTL135_F | 0.59 | 0.61 | 0.73 | 0.85 | 1.04 | 1.17 | 1.26 | 1.31 | 0.79 | 0.93 | 1.13 | 1.18 | ns |
| DIFF_SSTL15_F | 0.63 | 0.67 | 0.77 | 0.85 | 1.04 | 1.17 | 1.26 | 1.26 | 0.79 | 0.93 | 1.13 | 1.13 | ns |
| DIFF_SSTL18_I_F | 0.65 | 0.69 | 0.78 | 0.85 | 1.10 | 1.19 | 1.23 | 1.34 | 0.85 | 0.96 | 1.10 | 1.21 | ns |
| DIFF_SSTL18_II_F | 0.65 | 0.69 | 0.78 | 0.85 | 1.02 | 1.10 | 1.14 | 1.32 | 0.77 | 0.87 | 1.00 | 1.19 | ns |

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|-------------------------|-------------------|------------|------|------|-------------------|------------|------|------|-------------------|------------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | |
| LVDS | 0.75 | 0.79 | 0.92 | 0.96 | 1.05 | 1.17 | 1.24 | 1.26 | 0.88 | 1.01 | 1.08 | 1.10 | ns |
| HSUL_12_S | 0.69 | 0.72 | 0.82 | 0.98 | 1.65 | 1.84 | 2.05 | 2.05 | 1.48 | 1.68 | 1.89 | 1.89 | ns |
| HSUL_12_F | 0.69 | 0.72 | 0.82 | 0.98 | 1.39 | 1.54 | 1.68 | 1.68 | 1.22 | 1.38 | 1.52 | 1.52 | ns |
| DIFF_HSUL_12_S | 0.69 | 0.72 | 0.82 | 0.98 | 1.65 | 1.84 | 2.05 | 2.05 | 1.48 | 1.68 | 1.89 | 1.89 | ns |
| DIFF_HSUL_12_F | 0.69 | 0.72 | 0.82 | 0.98 | 1.39 | 1.54 | 1.68 | 1.68 | 1.22 | 1.38 | 1.52 | 1.52 | ns |
| DIFF_HSUL_12_DCI_S | 0.69 | 0.72 | 0.82 | 0.82 | 1.78 | 1.91 | 2.05 | 2.05 | 1.61 | 1.76 | 1.89 | 1.89 | ns |
| DIFF_HSUL_12_DCI_F | 0.69 | 0.72 | 0.82 | 0.82 | 1.56 | 1.67 | 1.76 | 1.76 | 1.39 | 1.51 | 1.60 | 1.60 | ns |
| HSTL_I_S | 0.68 | 0.72 | 0.82 | 0.90 | 1.15 | 1.28 | 1.38 | 1.38 | 0.98 | 1.12 | 1.22 | 1.22 | ns |
| HSTL_II_S | 0.68 | 0.72 | 0.82 | 0.90 | 1.05 | 1.17 | 1.26 | 1.27 | 0.88 | 1.01 | 1.10 | 1.11 | ns |
| HSTL_I_18_S | 0.70 | 0.72 | 0.82 | 0.95 | 1.12 | 1.24 | 1.34 | 1.34 | 0.95 | 1.08 | 1.18 | 1.18 | ns |
| HSTL_II_18_S | 0.70 | 0.72 | 0.82 | 0.90 | 1.06 | 1.18 | 1.26 | 1.27 | 0.89 | 1.02 | 1.10 | 1.11 | ns |
| HSTL_I_12_S | 0.68 | 0.72 | 0.82 | 0.96 | 1.14 | 1.27 | 1.37 | 1.37 | 0.97 | 1.11 | 1.21 | 1.21 | ns |
| HSTL_I_DCI_S | 0.68 | 0.72 | 0.82 | 0.90 | 1.11 | 1.23 | 1.33 | 1.33 | 0.94 | 1.07 | 1.17 | 1.17 | ns |
| HSTL_II_DCI_S | 0.68 | 0.72 | 0.82 | 0.85 | 1.05 | 1.17 | 1.26 | 1.26 | 0.88 | 1.01 | 1.10 | 1.10 | ns |
| HSTL_II_T_DCI_S | 0.70 | 0.72 | 0.82 | 0.82 | 1.15 | 1.28 | 1.38 | 1.38 | 0.98 | 1.12 | 1.22 | 1.22 | ns |
| HSTL_I_DCI_18_S | 0.70 | 0.72 | 0.82 | 0.90 | 1.11 | 1.23 | 1.33 | 1.33 | 0.94 | 1.07 | 1.17 | 1.17 | ns |
| HSTL_II_DCI_18_S | 0.70 | 0.72 | 0.82 | 0.82 | 1.05 | 1.16 | 1.24 | 1.24 | 0.88 | 1.00 | 1.08 | 1.08 | ns |
| HSTL_II_T_DCI_18_S | 0.70 | 0.72 | 0.82 | 0.84 | 1.11 | 1.23 | 1.33 | 1.34 | 0.94 | 1.07 | 1.17 | 1.18 | ns |
| DIFF_HSTL_I_S | 0.75 | 0.79 | 0.92 | 1.02 | 1.15 | 1.28 | 1.38 | 1.38 | 0.98 | 1.12 | 1.22 | 1.22 | ns |
| DIFF_HSTL_II_S | 0.75 | 0.79 | 0.92 | 1.02 | 1.05 | 1.17 | 1.26 | 1.32 | 0.88 | 1.01 | 1.10 | 1.16 | ns |
| DIFF_HSTL_I_DCI_S | 0.75 | 0.79 | 0.92 | 0.92 | 1.15 | 1.28 | 1.38 | 1.38 | 0.98 | 1.12 | 1.22 | 1.22 | ns |
| DIFF_HSTL_II_DCI_S | 0.75 | 0.79 | 0.92 | 0.92 | 1.05 | 1.17 | 1.26 | 1.26 | 0.88 | 1.01 | 1.10 | 1.10 | ns |
| DIFF_HSTL_I_18_S | 0.75 | 0.79 | 0.92 | 0.98 | 1.12 | 1.24 | 1.34 | 1.34 | 0.95 | 1.08 | 1.18 | 1.18 | ns |
| DIFF_HSTL_II_18_S | 0.75 | 0.79 | 0.92 | 0.99 | 1.06 | 1.18 | 1.26 | 1.32 | 0.89 | 1.02 | 1.10 | 1.16 | ns |
| DIFF_HSTL_I_DCI_18_S | 0.75 | 0.79 | 0.92 | 0.92 | 1.11 | 1.23 | 1.33 | 1.33 | 0.94 | 1.07 | 1.17 | 1.17 | ns |
| DIFF_HSTL_II_DCI_18_S | 0.75 | 0.79 | 0.92 | 0.93 | 1.05 | 1.16 | 1.24 | 1.26 | 0.88 | 1.00 | 1.08 | 1.10 | ns |
| DIFF_HSTL_II_T_DCI_18_S | 0.75 | 0.79 | 0.92 | 0.92 | 1.11 | 1.23 | 1.33 | 1.33 | 0.94 | 1.07 | 1.17 | 1.17 | ns |
| HSTL_I_F | 0.68 | 0.72 | 0.82 | 0.90 | 1.02 | 1.14 | 1.22 | 1.22 | 0.85 | 0.98 | 1.06 | 1.06 | ns |
| HSTL_II_F | 0.68 | 0.72 | 0.82 | 0.90 | 0.97 | 1.08 | 1.15 | 1.15 | 0.80 | 0.92 | 0.99 | 0.99 | ns |
| HSTL_I_18_F | 0.70 | 0.72 | 0.82 | 0.95 | 1.04 | 1.16 | 1.24 | 1.24 | 0.87 | 1.00 | 1.08 | 1.08 | ns |
| HSTL_II_18_F | 0.70 | 0.72 | 0.82 | 0.90 | 0.98 | 1.09 | 1.16 | 1.20 | 0.81 | 0.94 | 1.00 | 1.03 | ns |
| HSTL_I_12_F | 0.68 | 0.72 | 0.82 | 0.96 | 1.02 | 1.13 | 1.21 | 1.21 | 0.85 | 0.97 | 1.05 | 1.05 | ns |
| HSTL_I_DCI_F | 0.68 | 0.72 | 0.82 | 0.90 | 1.04 | 1.16 | 1.24 | 1.24 | 0.87 | 1.00 | 1.08 | 1.08 | ns |
| HSTL_II_DCI_F | 0.68 | 0.72 | 0.82 | 0.85 | 0.97 | 1.08 | 1.15 | 1.15 | 0.80 | 0.92 | 0.99 | 0.99 | ns |
| HSTL_II_T_DCI_F | 0.70 | 0.72 | 0.82 | 0.82 | 1.02 | 1.14 | 1.22 | 1.22 | 0.85 | 0.98 | 1.06 | 1.06 | ns |
| HSTL_I_DCI_18_F | 0.70 | 0.72 | 0.82 | 0.90 | 1.04 | 1.16 | 1.24 | 1.24 | 0.87 | 1.00 | 1.08 | 1.08 | ns |
| HSTL_II_DCI_18_F | 0.70 | 0.72 | 0.82 | 0.82 | 0.98 | 1.09 | 1.16 | 1.16 | 0.81 | 0.93 | 1.00 | 1.00 | ns |
| HSTL_II_T_DCI_18_F | 0.70 | 0.72 | 0.82 | 0.84 | 1.04 | 1.16 | 1.24 | 1.24 | 0.87 | 1.00 | 1.08 | 1.08 | ns |
| DIFF_HSTL_I_F | 0.75 | 0.79 | 0.92 | 1.02 | 1.02 | 1.14 | 1.22 | 1.22 | 0.85 | 0.98 | 1.06 | 1.06 | ns |

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|-------------------------|-------------------|------------|------|------|-------------------|------------|------|------|-------------------|------------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | |
| DIFF_HSTL_II_F | 0.75 | 0.79 | 0.92 | 1.02 | 0.97 | 1.08 | 1.15 | 1.20 | 0.80 | 0.92 | 0.99 | 1.03 | ns |
| DIFF_HSTL_I_DCI_F | 0.75 | 0.79 | 0.92 | 0.92 | 1.02 | 1.14 | 1.22 | 1.22 | 0.85 | 0.98 | 1.06 | 1.06 | ns |
| DIFF_HSTL_II_DCI_F | 0.75 | 0.79 | 0.92 | 0.92 | 0.97 | 1.08 | 1.15 | 1.15 | 0.80 | 0.92 | 0.99 | 0.99 | ns |
| DIFF_HSTL_I_18_F | 0.75 | 0.79 | 0.92 | 0.98 | 1.04 | 1.16 | 1.24 | 1.24 | 0.87 | 1.00 | 1.08 | 1.08 | ns |
| DIFF_HSTL_II_18_F | 0.75 | 0.79 | 0.92 | 0.99 | 0.98 | 1.09 | 1.16 | 1.24 | 0.81 | 0.94 | 1.00 | 1.08 | ns |
| DIFF_HSTL_I_DCI_18_F | 0.75 | 0.79 | 0.92 | 0.92 | 1.04 | 1.16 | 1.24 | 1.24 | 0.87 | 1.00 | 1.08 | 1.08 | ns |
| DIFF_HSTL_II_DCI_18_F | 0.75 | 0.79 | 0.92 | 0.93 | 0.98 | 1.09 | 1.16 | 1.18 | 0.81 | 0.93 | 1.00 | 1.02 | ns |
| DIFF_HSTL_II_T_DCI_18_F | 0.75 | 0.79 | 0.92 | 0.92 | 1.04 | 1.16 | 1.24 | 1.24 | 0.87 | 1.00 | 1.08 | 1.08 | ns |
| LVC MOS18_S2 | 0.47 | 0.50 | 0.60 | 0.90 | 3.95 | 4.28 | 4.85 | 4.85 | 3.78 | 4.13 | 4.69 | 4.69 | ns |
| LVC MOS18_S4 | 0.47 | 0.50 | 0.60 | 0.90 | 2.67 | 2.98 | 3.43 | 3.43 | 2.50 | 2.82 | 3.27 | 3.27 | ns |
| LVC MOS18_S6 | 0.47 | 0.50 | 0.60 | 0.90 | 2.14 | 2.38 | 2.72 | 2.72 | 1.97 | 2.22 | 2.56 | 2.56 | ns |
| LVC MOS18_S8 | 0.47 | 0.50 | 0.60 | 0.90 | 1.98 | 2.21 | 2.52 | 2.52 | 1.81 | 2.05 | 2.36 | 2.36 | ns |
| LVC MOS18_S12 | 0.47 | 0.50 | 0.60 | 0.90 | 1.70 | 1.91 | 2.17 | 2.17 | 1.53 | 1.75 | 2.01 | 2.01 | ns |
| LVC MOS18_S16 | 0.47 | 0.50 | 0.60 | 0.90 | 1.57 | 1.75 | 1.97 | 1.97 | 1.40 | 1.59 | 1.81 | 1.81 | ns |
| LVC MOS18_F2 | 0.47 | 0.50 | 0.60 | 0.90 | 3.50 | 3.87 | 4.48 | 4.48 | 3.33 | 3.71 | 4.32 | 4.32 | ns |
| LVC MOS18_F4 | 0.47 | 0.50 | 0.60 | 0.90 | 2.23 | 2.50 | 2.87 | 2.87 | 2.06 | 2.34 | 2.71 | 2.71 | ns |
| LVC MOS18_F6 | 0.47 | 0.50 | 0.60 | 0.90 | 1.80 | 2.00 | 2.26 | 2.26 | 1.63 | 1.84 | 2.09 | 2.09 | ns |
| LVC MOS18_F8 | 0.47 | 0.50 | 0.60 | 0.90 | 1.46 | 1.72 | 2.04 | 2.04 | 1.29 | 1.56 | 1.88 | 1.88 | ns |
| LVC MOS18_F12 | 0.47 | 0.50 | 0.60 | 0.90 | 1.26 | 1.40 | 1.53 | 1.53 | 1.09 | 1.24 | 1.37 | 1.37 | ns |
| LVC MOS18_F16 | 0.47 | 0.50 | 0.60 | 0.90 | 1.19 | 1.33 | 1.44 | 1.66 | 1.02 | 1.17 | 1.28 | 1.50 | ns |
| LVC MOS15_S2 | 0.59 | 0.62 | 0.73 | 0.88 | 3.55 | 3.89 | 4.45 | 4.45 | 3.38 | 3.73 | 4.29 | 4.29 | ns |
| LVC MOS15_S4 | 0.59 | 0.62 | 0.73 | 0.88 | 2.45 | 2.70 | 3.06 | 3.06 | 2.28 | 2.54 | 2.90 | 2.90 | ns |
| LVC MOS15_S6 | 0.59 | 0.62 | 0.73 | 0.88 | 2.24 | 2.51 | 2.88 | 2.88 | 2.07 | 2.35 | 2.72 | 2.72 | ns |
| LVC MOS15_S8 | 0.59 | 0.62 | 0.73 | 0.88 | 1.91 | 2.16 | 2.49 | 2.49 | 1.74 | 2.00 | 2.32 | 2.32 | ns |
| LVC MOS15_S12 | 0.59 | 0.62 | 0.73 | 0.88 | 1.77 | 1.98 | 2.23 | 2.23 | 1.60 | 1.82 | 2.07 | 2.07 | ns |
| LVC MOS15_S16 | 0.59 | 0.62 | 0.73 | 0.88 | 1.62 | 1.81 | 2.02 | 2.02 | 1.45 | 1.65 | 1.86 | 1.86 | ns |
| LVC MOS15_F2 | 0.59 | 0.62 | 0.73 | 0.88 | 3.38 | 3.69 | 4.18 | 4.18 | 3.21 | 3.53 | 4.02 | 4.02 | ns |
| LVC MOS15_F4 | 0.59 | 0.62 | 0.73 | 0.88 | 2.04 | 2.21 | 2.44 | 2.44 | 1.87 | 2.06 | 2.27 | 2.27 | ns |
| LVC MOS15_F6 | 0.59 | 0.62 | 0.73 | 0.88 | 1.47 | 1.74 | 2.09 | 2.09 | 1.30 | 1.58 | 1.93 | 1.93 | ns |
| LVC MOS15_F8 | 0.59 | 0.62 | 0.73 | 0.88 | 1.31 | 1.46 | 1.61 | 1.61 | 1.14 | 1.30 | 1.45 | 1.45 | ns |
| LVC MOS15_F12 | 0.59 | 0.62 | 0.73 | 0.88 | 1.21 | 1.34 | 1.45 | 1.45 | 1.04 | 1.18 | 1.29 | 1.29 | ns |
| LVC MOS15_F16 | 0.59 | 0.62 | 0.73 | 0.88 | 1.18 | 1.31 | 1.41 | 1.68 | 1.01 | 1.15 | 1.25 | 1.52 | ns |
| LVC MOS12_S2 | 0.64 | 0.67 | 0.78 | 1.04 | 3.38 | 3.80 | 4.48 | 4.48 | 3.21 | 3.64 | 4.31 | 4.31 | ns |
| LVC MOS12_S4 | 0.64 | 0.67 | 0.78 | 1.04 | 2.62 | 2.94 | 3.43 | 3.43 | 2.45 | 2.78 | 3.27 | 3.27 | ns |
| LVC MOS12_S6 | 0.64 | 0.67 | 0.78 | 1.04 | 2.05 | 2.33 | 2.72 | 2.72 | 1.88 | 2.17 | 2.56 | 2.56 | ns |
| LVC MOS12_S8 | 0.64 | 0.67 | 0.78 | 1.04 | 1.94 | 2.18 | 2.51 | 2.51 | 1.77 | 2.02 | 2.34 | 2.34 | ns |
| LVC MOS12_F2 | 0.64 | 0.67 | 0.78 | 1.04 | 2.84 | 3.15 | 3.62 | 3.62 | 2.67 | 2.99 | 3.46 | 3.46 | ns |
| LVC MOS12_F4 | 0.64 | 0.67 | 0.78 | 1.04 | 1.97 | 2.18 | 2.44 | 2.44 | 1.80 | 2.02 | 2.28 | 2.28 | ns |
| LVC MOS12_F6 | 0.64 | 0.67 | 0.78 | 1.04 | 1.33 | 1.51 | 1.70 | 1.70 | 1.16 | 1.35 | 1.54 | 1.54 | ns |
| LVC MOS12_F8 | 0.64 | 0.67 | 0.78 | 1.04 | 1.27 | 1.42 | 1.55 | 1.55 | 1.10 | 1.26 | 1.39 | 1.39 | ns |

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|------------------------|-------------------|------------|------|------|-------------------|------------|------|------|-------------------|------------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | |
| LVDCI_18 | 0.47 | 0.50 | 0.60 | 0.87 | 1.99 | 2.15 | 2.35 | 2.35 | 1.82 | 1.99 | 2.19 | 2.19 | ns |
| LVDCI_15 | 0.59 | 0.62 | 0.73 | 0.92 | 1.98 | 2.23 | 2.58 | 2.58 | 1.81 | 2.07 | 2.41 | 2.41 | ns |
| LVDCI_DV2_18 | 0.47 | 0.50 | 0.60 | 0.88 | 1.99 | 2.15 | 2.34 | 2.34 | 1.82 | 1.99 | 2.18 | 2.18 | ns |
| LVDCI_DV2_15 | 0.59 | 0.62 | 0.73 | 0.88 | 1.98 | 2.23 | 2.58 | 2.58 | 1.81 | 2.07 | 2.41 | 2.41 | ns |
| HSLVDCI_18 | 0.68 | 0.72 | 0.82 | 0.90 | 1.99 | 2.15 | 2.35 | 2.35 | 1.82 | 1.99 | 2.19 | 2.19 | ns |
| HSLVDCI_15 | 0.68 | 0.72 | 0.82 | 0.93 | 1.98 | 2.23 | 2.58 | 2.58 | 1.81 | 2.07 | 2.41 | 2.41 | ns |
| SSTL18_I_S | 0.68 | 0.72 | 0.82 | 0.95 | 1.02 | 1.15 | 1.24 | 1.24 | 0.85 | 0.99 | 1.08 | 1.08 | ns |
| SSTL18_II_S | 0.68 | 0.72 | 0.82 | 1.01 | 1.17 | 1.29 | 1.37 | 1.38 | 1.00 | 1.13 | 1.21 | 1.22 | ns |
| SSTL18_I_DCI_S | 0.68 | 0.72 | 0.82 | 0.87 | 0.92 | 1.06 | 1.17 | 1.18 | 0.75 | 0.90 | 1.01 | 1.02 | ns |
| SSTL18_II_DCI_S | 0.68 | 0.72 | 0.82 | 0.82 | 0.88 | 0.98 | 1.08 | 1.12 | 0.71 | 0.83 | 0.92 | 0.96 | ns |
| SSTL18_II_T_DCI_S | 0.68 | 0.72 | 0.82 | 0.98 | 0.92 | 1.06 | 1.17 | 1.18 | 0.75 | 0.90 | 1.01 | 1.02 | ns |
| SSTL15_S | 0.68 | 0.72 | 0.82 | 0.82 | 0.94 | 1.06 | 1.15 | 1.16 | 0.77 | 0.91 | 0.99 | 1.00 | ns |
| SSTL15_DCI_S | 0.68 | 0.72 | 0.82 | 0.90 | 0.94 | 1.06 | 1.15 | 1.16 | 0.77 | 0.90 | 0.99 | 1.00 | ns |
| SSTL15_T_DCI_S | 0.68 | 0.72 | 0.82 | 0.87 | 0.94 | 1.06 | 1.15 | 1.15 | 0.77 | 0.90 | 0.99 | 0.99 | ns |
| SSTL135_S | 0.69 | 0.72 | 0.82 | 0.93 | 0.97 | 1.10 | 1.19 | 1.20 | 0.80 | 0.94 | 1.03 | 1.03 | ns |
| SSTL135_DCI_S | 0.69 | 0.72 | 0.82 | 0.85 | 0.97 | 1.09 | 1.19 | 1.20 | 0.80 | 0.93 | 1.03 | 1.03 | ns |
| SSTL135_T_DCI_S | 0.69 | 0.72 | 0.82 | 0.93 | 0.97 | 1.09 | 1.19 | 1.20 | 0.80 | 0.93 | 1.03 | 1.03 | ns |
| SSTL12_S | 0.69 | 0.72 | 0.82 | 1.02 | 0.96 | 1.09 | 1.18 | 1.18 | 0.79 | 0.93 | 1.02 | 1.02 | ns |
| SSTL12_DCI_S | 0.69 | 0.72 | 0.82 | 0.90 | 1.03 | 1.17 | 1.27 | 1.27 | 0.86 | 1.01 | 1.11 | 1.11 | ns |
| SSTL12_T_DCI_S | 0.69 | 0.72 | 0.82 | 0.88 | 1.03 | 1.17 | 1.27 | 1.27 | 0.86 | 1.01 | 1.11 | 1.11 | ns |
| DIFF_SSTL18_I_S | 0.75 | 0.79 | 0.92 | 0.99 | 1.02 | 1.15 | 1.24 | 1.29 | 0.85 | 0.99 | 1.08 | 1.13 | ns |
| DIFF_SSTL18_II_S | 0.75 | 0.79 | 0.92 | 0.93 | 1.17 | 1.29 | 1.37 | 1.40 | 1.00 | 1.13 | 1.21 | 1.24 | ns |
| DIFF_SSTL18_I_DCI_S | 0.75 | 0.79 | 0.92 | 0.92 | 0.92 | 1.06 | 1.17 | 1.24 | 0.75 | 0.90 | 1.01 | 1.08 | ns |
| DIFF_SSTL18_II_DCI_S | 0.75 | 0.79 | 0.92 | 0.96 | 0.88 | 0.98 | 1.08 | 1.18 | 0.71 | 0.83 | 0.92 | 1.02 | ns |
| DIFF_SSTL18_II_T_DCI_S | 0.75 | 0.79 | 0.92 | 0.92 | 0.92 | 1.06 | 1.17 | 1.24 | 0.75 | 0.90 | 1.01 | 1.08 | ns |
| DIFF_SSTL15_S | 0.68 | 0.72 | 0.82 | 0.99 | 0.94 | 1.06 | 1.15 | 1.16 | 0.77 | 0.91 | 0.99 | 1.00 | ns |
| DIFF_SSTL15_DCI_S | 0.68 | 0.72 | 0.82 | 0.96 | 0.94 | 1.06 | 1.15 | 1.16 | 0.77 | 0.90 | 0.99 | 1.00 | ns |
| DIFF_SSTL15_T_DCI_S | 0.68 | 0.72 | 0.82 | 0.88 | 0.94 | 1.06 | 1.15 | 1.23 | 0.77 | 0.90 | 0.99 | 1.07 | ns |
| DIFF_SSTL135_S | 0.69 | 0.72 | 0.82 | 1.09 | 0.97 | 1.10 | 1.19 | 1.20 | 0.80 | 0.94 | 1.03 | 1.03 | ns |
| DIFF_SSTL135_DCI_S | 0.69 | 0.72 | 0.82 | 0.90 | 0.97 | 1.09 | 1.19 | 1.20 | 0.80 | 0.93 | 1.03 | 1.03 | ns |
| DIFF_SSTL135_T_DCI_S | 0.69 | 0.72 | 0.82 | 0.84 | 0.97 | 1.09 | 1.19 | 1.27 | 0.80 | 0.93 | 1.03 | 1.11 | ns |
| DIFF_SSTL12_S | 0.69 | 0.72 | 0.82 | 0.96 | 0.96 | 1.09 | 1.18 | 1.18 | 0.79 | 0.93 | 1.02 | 1.02 | ns |
| DIFF_SSTL12_DCI_S | 0.69 | 0.72 | 0.82 | 0.87 | 1.03 | 1.17 | 1.27 | 1.27 | 0.86 | 1.01 | 1.11 | 1.11 | ns |
| DIFF_SSTL12_T_DCI_S | 0.69 | 0.72 | 0.82 | 0.96 | 1.03 | 1.17 | 1.27 | 1.27 | 0.86 | 1.01 | 1.11 | 1.11 | ns |
| SSTL18_I_F | 0.68 | 0.72 | 0.82 | 0.95 | 0.94 | 1.06 | 1.15 | 1.15 | 0.77 | 0.91 | 0.99 | 0.99 | ns |
| SSTL18_II_F | 0.68 | 0.72 | 0.82 | 1.01 | 0.97 | 1.09 | 1.16 | 1.21 | 0.80 | 0.93 | 1.00 | 1.05 | ns |
| SSTL18_I_DCI_F | 0.68 | 0.72 | 0.82 | 0.87 | 0.89 | 1.02 | 1.10 | 1.15 | 0.72 | 0.86 | 0.94 | 0.99 | ns |
| SSTL18_II_DCI_F | 0.68 | 0.72 | 0.82 | 0.82 | 0.89 | 1.02 | 1.10 | 1.10 | 0.72 | 0.86 | 0.94 | 0.94 | ns |
| SSTL18_II_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.98 | 0.89 | 1.02 | 1.10 | 1.15 | 0.72 | 0.86 | 0.94 | 0.99 | ns |
| SSTL15_F | 0.68 | 0.72 | 0.82 | 0.82 | 0.89 | 1.01 | 1.09 | 1.09 | 0.72 | 0.85 | 0.93 | 0.93 | ns |

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|------------------------|-------------------|------------|------|------|-------------------|------------|------|------|-------------------|------------|------|------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | -3 | -2/-2L/-2G | -1 | -1M | |
| SSTL15_DCI_F | 0.68 | 0.72 | 0.82 | 0.90 | 0.89 | 1.01 | 1.09 | 1.12 | 0.72 | 0.85 | 0.93 | 0.96 | ns |
| SSTL15_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.87 | 0.89 | 1.01 | 1.09 | 1.12 | 0.72 | 0.85 | 0.93 | 0.96 | ns |
| SSTL135_F | 0.69 | 0.72 | 0.82 | 0.93 | 0.88 | 1.00 | 1.08 | 1.12 | 0.71 | 0.85 | 0.92 | 0.96 | ns |
| SSTL135_DCI_F | 0.69 | 0.72 | 0.82 | 0.85 | 0.89 | 1.00 | 1.08 | 1.12 | 0.72 | 0.85 | 0.92 | 0.96 | ns |
| SSTL135_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.93 | 0.89 | 1.00 | 1.08 | 1.12 | 0.72 | 0.85 | 0.92 | 0.96 | ns |
| SSTL12_F | 0.69 | 0.72 | 0.82 | 1.02 | 0.88 | 1.00 | 1.08 | 1.12 | 0.71 | 0.84 | 0.92 | 0.96 | ns |
| SSTL12_DCI_F | 0.69 | 0.72 | 0.82 | 0.90 | 0.91 | 1.03 | 1.11 | 1.11 | 0.74 | 0.88 | 0.95 | 0.95 | ns |
| SSTL12_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.88 | 0.91 | 1.03 | 1.11 | 1.12 | 0.74 | 0.88 | 0.95 | 0.96 | ns |
| DIFF_SSTL18_I_F | 0.75 | 0.79 | 0.92 | 0.99 | 0.94 | 1.06 | 1.15 | 1.23 | 0.77 | 0.91 | 0.99 | 1.07 | ns |
| DIFF_SSTL18_II_F | 0.75 | 0.79 | 0.92 | 0.93 | 0.97 | 1.09 | 1.16 | 1.24 | 0.80 | 0.93 | 1.00 | 1.08 | ns |
| DIFF_SSTL18_I_DCI_F | 0.75 | 0.79 | 0.92 | 0.92 | 0.89 | 1.02 | 1.10 | 1.23 | 0.72 | 0.86 | 0.94 | 1.07 | ns |
| DIFF_SSTL18_II_DCI_F | 0.75 | 0.79 | 0.92 | 0.96 | 0.89 | 1.02 | 1.10 | 1.16 | 0.72 | 0.86 | 0.94 | 1.00 | ns |
| DIFF_SSTL18_II_T_DCI_F | 0.75 | 0.79 | 0.92 | 0.92 | 0.89 | 1.02 | 1.10 | 1.24 | 0.72 | 0.86 | 0.94 | 1.08 | ns |
| DIFF_SSTL15_F | 0.68 | 0.72 | 0.82 | 0.99 | 0.89 | 1.01 | 1.09 | 1.09 | 0.72 | 0.85 | 0.93 | 0.93 | ns |
| DIFF_SSTL15_DCI_F | 0.68 | 0.72 | 0.82 | 0.96 | 0.89 | 1.01 | 1.09 | 1.12 | 0.72 | 0.85 | 0.93 | 0.96 | ns |
| DIFF_SSTL15_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.88 | 0.89 | 1.01 | 1.09 | 1.20 | 0.72 | 0.85 | 0.93 | 1.03 | ns |
| DIFF_SSTL135_F | 0.69 | 0.72 | 0.82 | 1.09 | 0.88 | 1.00 | 1.08 | 1.12 | 0.71 | 0.85 | 0.92 | 0.96 | ns |
| DIFF_SSTL135_DCI_F | 0.69 | 0.72 | 0.82 | 0.90 | 0.89 | 1.00 | 1.08 | 1.12 | 0.72 | 0.85 | 0.92 | 0.96 | ns |
| DIFF_SSTL135_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.84 | 0.89 | 1.00 | 1.08 | 1.20 | 0.72 | 0.85 | 0.92 | 1.03 | ns |
| DIFF_SSTL12_F | 0.69 | 0.72 | 0.82 | 0.96 | 0.88 | 1.00 | 1.08 | 1.12 | 0.71 | 0.84 | 0.92 | 0.96 | ns |
| DIFF_SSTL12_DCI_F | 0.69 | 0.72 | 0.82 | 0.87 | 0.91 | 1.03 | 1.11 | 1.11 | 0.74 | 0.88 | 0.95 | 0.95 | ns |
| DIFF_SSTL12_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.96 | 0.91 | 1.03 | 1.11 | 1.18 | 0.74 | 0.88 | 0.95 | 1.02 | ns |

Table 21 specifies the values of T_{IOTPHZ} and T_{IOIBUFDISABLE}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{IOIBUFDISABLE} is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: IOB 3-state Output Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------------|---|-------------|------------|------|------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| T _{IOTPHZ} | T input to pad high-impedance | 0.76 | 0.86 | 0.99 | 0.99 | ns |
| T _{IOIBUFDISABLE_HR} | IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks | 1.72 | 1.89 | 2.14 | 2.14 | ns |
| T _{IOIBUFDISABLE_HP} | IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks | 1.31 | 1.46 | 1.76 | 1.76 | ns |

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 22 shows the test setup parameters used for measuring input delay.

Table 22: Input Delay Measurement Methodology

| Description | I/O Standard Attribute | $V_L^{(1)(2)}$ | $V_H^{(1)(2)}$ | $V_{MEAS}^{(1)(4)(6)}$ | $V_{REF}^{(1)(3)(5)}$ |
|--|---------------------------------|-------------------|-------------------|------------------------|-----------------------|
| LVC MOS, 1.2V | LVC MOS12 | 0.1 | 1.1 | 0.6 | – |
| LVC MOS, 1.5V | LVC MOS15 | 0.1 | 1.4 | 0.75 | – |
| LVC MOS, 1.8V | LVC MOS18 | 0.1 | 1.7 | 0.9 | – |
| LVC MOS, 2.5V | LVC MOS25 | 0.1 | 2.4 | 1.25 | – |
| LVC MOS, 3.3V | LVC MOS33 | 0.1 | 3.2 | 1.65 | – |
| LV TTL, 3.3V | LV TTL | 0.1 | 3.2 | 1.65 | – |
| MOBILE_DDR, 1.8V | MOBILE_DDR | 0.1 | 1.7 | 0.9 | – |
| PCI33, 3.3V | PCI33_3 | 0.1 | 3.2 | 1.65 | – |
| HSTL (High-Speed Transceiver Logic), Class I, 1.2V | HSTL_I_12 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.60 |
| HSTL, Class I & II, 1.5V | HSTL_I, HSTL_II | $V_{REF} - 0.65$ | $V_{REF} + 0.65$ | V_{REF} | 0.75 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF} - 0.8$ | $V_{REF} + 0.8$ | V_{REF} | 0.90 |
| HSUL (High-Speed Unterminated Logic), 1.2V | HSUL_12 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.60 |
| SSTL (Stub Terminated Transceiver Logic), 1.2V | SSTL12 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.60 |
| SSTL, 1.35V | SSTL135, SSTL135_R | $V_{REF} - 0.575$ | $V_{REF} + 0.575$ | V_{REF} | 0.675 |
| SSTL, 1.5V | SSTL15, SSTL15_R | $V_{REF} - 0.65$ | $V_{REF} + 0.65$ | V_{REF} | 0.75 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF} - 0.8$ | $V_{REF} + 0.8$ | V_{REF} | 0.90 |
| DIFF_MOBILE_DDR, 1.8V | DIFF_MOBILE_DDR | $0.9 - 0.125$ | $0.9 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_HSTL, Class I, 1.2V | DIFF_HSTL_I_12 | $0.6 - 0.125$ | $0.6 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_HSTL, Class I & II, 1.5V | DIFF_HSTL_I, DIFF_HSTL_II | $0.75 - 0.125$ | $0.75 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_HSTL, Class I & II, 1.8V | DIFF_HSTL_I_18, DIFF_HSTL_II_18 | $0.9 - 0.125$ | $0.9 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | $0.6 - 0.125$ | $0.6 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_SSTL, 1.2V | DIFF_SSTL12 | $0.6 - 0.125$ | $0.6 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_SSTL135/DIFF_SSTL135_R, 1.35V | DIFF_SSTL135, DIFF_SSTL135_R | $0.675 - 0.125$ | $0.675 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_SSTL15/DIFF_SSTL15_R, 1.5V | DIFF_SSTL15, DIFF_SSTL15_R | $0.75 - 0.125$ | $0.75 + 0.125$ | 0 ⁽⁶⁾ | – |
| DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | $0.9 - 0.125$ | $0.9 + 0.125$ | 0 ⁽⁶⁾ | – |
| LVDS (Low-Voltage Differential Signaling), 1.8V | LVDS | $0.9 - 0.125$ | $0.9 + 0.125$ | 0 ⁽⁶⁾ | – |
| LVDS_25, 2.5V | LVDS_25 | $1.2 - 0.125$ | $1.2 + 0.125$ | 0 ⁽⁶⁾ | – |
| BLVDS_25, 2.5V | BLVDS_25 | $1.25 - 0.125$ | $1.25 + 0.125$ | 0 ⁽⁶⁾ | – |
| MINI_LVDS_25, 2.5V | MINI_LVDS_25 | $1.25 - 0.125$ | $1.25 + 0.125$ | 0 ⁽⁶⁾ | – |
| PPDS_25 | PPDS_25 | $1.25 - 0.125$ | $1.25 + 0.125$ | 0 ⁽⁶⁾ | – |
| RS DS_25 | RS DS_25 | $1.25 - 0.125$ | $1.25 + 0.125$ | 0 ⁽⁶⁾ | – |

Table 22: Input Delay Measurement Methodology (Cont'd)

| Description | I/O Standard Attribute | V_L (1)(2) | V_H (1)(2) | V_{MEAS} (1)(4)(6) | V_{REF} (1)(3)(5) |
|-------------|------------------------|--------------|--------------|----------------------|---------------------|
| TMDS_33 | TMDS_33 | 3 - 0.125 | 3 + 0.125 | 0 ⁽⁶⁾ | - |

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

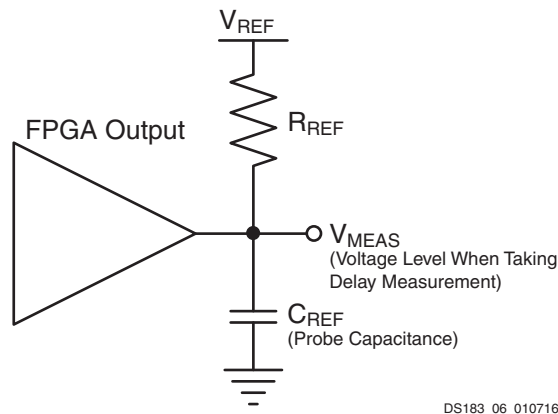


Figure 1: Single-Ended Test Setup

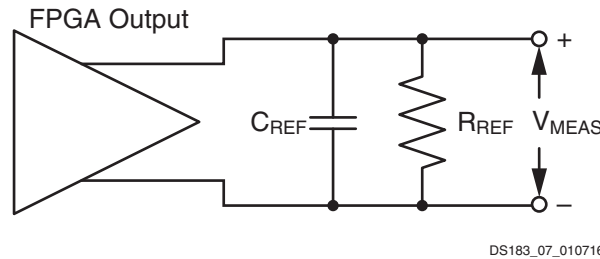


Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 23.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .

5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 23: Output Delay Measurement Methodology

| Description | I/O Standard Attribute | R _{REF} (Ω) | C _{REF} ⁽¹⁾ (pF) | V _{MEAS} (V) | V _{REF} (V) |
|---|---------------------------------|----------------------|--------------------------------------|-----------------------|----------------------|
| LVC MOS, 1.2V | LVC MOS12 | 1M | 0 | 0.6 | 0 |
| LVC MOS/LVDCI/HSLVDCI, 1.5V | LVC MOS15, LVDCI_15, HSLVDCI_15 | 1M | 0 | 0.75 | 0 |
| LVC MOS/LVDCI/HSLVDCI, 1.8V | LVC MOS18, LVDCI_15, HSLVDCI_18 | 1M | 0 | 0.9 | 0 |
| LVC MOS, 2.5V | LVC MOS25 | 1M | 0 | 1.25 | 0 |
| LVC MOS, 3.3V | LVC MOS33 | 1M | 0 | 1.65 | 0 |
| LV TTL, 3.3V | LV TTL | 1M | 0 | 1.65 | 0 |
| PCI33, 3.3V | PCI33_3 | 25 | 10 | 1.65 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I, 1.2V | HSTL_I_12 | 50 | 0 | V _{REF} | 0.6 |
| HSTL, Class I, 1.5V | HSTL_I | 50 | 0 | V _{REF} | 0.75 |
| HSTL, Class II, 1.5V | HSTL_II | 25 | 0 | V _{REF} | 0.75 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | V _{REF} | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | V _{REF} | 0.9 |
| HSUL (High-Speed Unterminated Logic), 1.2V | HSUL_12 | 50 | 0 | V _{REF} | 0.6 |
| SSTL12, 1.2V | SSTL12 | 50 | 0 | V _{REF} | 0.6 |
| SSTL135/SSTL135_R, 1.35V | SSTL135, SSTL135_R | 50 | 0 | V _{REF} | 0.675 |
| SSTL15/SSTL15_R, 1.5V | SSTL15, SSTL15_R | 50 | 0 | V _{REF} | 0.75 |
| SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V | SSTL18_I, SSTL18_II | 50 | 0 | V _{REF} | 0.9 |
| DIFF_MOBILE_DDR, 1.8V | DIFF_MOBILE_DDR | 50 | 0 | V _{REF} | 0.9 |
| DIFF_HSTL, Class I, 1.2V | DIFF_HSTL_I_12 | 50 | 0 | V _{REF} | 0.6 |
| DIFF_HSTL, Class I & II, 1.5V | DIFF_HSTL_I, DIFF_HSTL_II | 50 | 0 | V _{REF} | 0.75 |
| DIFF_HSTL, Class I & II, 1.8V | DIFF_HSTL_I_18, DIFF_HSTL_II_18 | 50 | 0 | V _{REF} | 0.9 |
| DIFF_HSUL_12, 1.2V | DIFF_HSUL_12 | 50 | 0 | V _{REF} | 0.6 |
| DIFF_SSTL12, 1.2V | DIFF_SSTL12 | 50 | 0 | V _{REF} | 0.6 |
| DIFF_SSTL135/DIFF_SSTL135_R, 1.35V | DIFF_SSTL135, DIFF_SSTL135_R | 50 | 0 | V _{REF} | 0.675 |
| DIFF_SSTL15/DIFF_SSTL15_R, 1.5V | DIFF_SSTL15, DIFF_SSTL15_R | 50 | 0 | V _{REF} | 0.75 |
| DIFF_SSTL18, Class I & II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 50 | 0 | V _{REF} | 0.9 |
| LVDS (Low-Voltage Differential Signaling), 1.8V | LVDS | 100 | 0 | 0 ⁽²⁾ | 0 |
| LVDS, 2.5V | LVDS_25 | 100 | 0 | 0 ⁽²⁾ | 0 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 100 | 0 | 0 ⁽²⁾ | 0 |
| Mini LVDS, 2.5V | MINI_LVDS_25 | 100 | 0 | 0 ⁽²⁾ | 0 |
| PPDS_25 | PPDS_25 | 100 | 0 | 0 ⁽²⁾ | 0 |
| RS DS_25 | RS DS_25 | 100 | 0 | 0 ⁽²⁾ | 0 |
| TMDS_33 | TMDS_33 | 50 | 0 | 0 ⁽²⁾ | 3.3 |

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 24: ILOGIC Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|-----------------------------|---|-------------|------------|-----------|-----------|---------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Setup/Hold | | | | | | |
| T_{ICE1CK}/T_{ICKCE1} | CE1 pin setup/hold with respect to CLK | 0.42/0.00 | 0.48/0.00 | 0.67/0.00 | 0.67/0.00 | ns |
| T_{ISRCK}/T_{ICKSR} | SR pin setup/hold with respect to CLK | 0.53/0.01 | 0.61/0.01 | 0.99/0.01 | 0.99/0.01 | ns |
| $T_{IDOCKE2}/T_{IOCKDE2}$ | D pin setup/hold with respect to CLK without delay (HP I/O banks only) | 0.01/0.27 | 0.01/0.29 | 0.01/0.34 | 0.01/0.34 | ns |
| $T_{IDOCKDE2}/T_{IOCKDDE2}$ | DDL pin setup/hold with respect to CLK (using IDELAY) (HP I/O banks only) | 0.01/0.27 | 0.02/0.29 | 0.02/0.34 | 0.02/0.34 | ns |
| $T_{IDOCKE3}/T_{IOCKDE3}$ | D pin setup/hold with respect to CLK without delay (HR I/O banks only) | 0.01/0.27 | 0.01/0.29 | 0.01/0.34 | 0.01/0.34 | ns |
| $T_{IDOCKDE3}/T_{IOCKDDE3}$ | DDL pin setup/hold with respect to CLK (using IDELAY) (HR I/O banks only) | 0.01/0.27 | 0.02/0.29 | 0.02/0.34 | 0.02/0.34 | ns |
| Combinatorial | | | | | | |
| T_{IDIE2} | D pin to O pin propagation delay, no delay (HP I/O banks only) | 0.09 | 0.10 | 0.12 | 0.12 | ns |
| T_{IDIDE2} | DDL pin to O pin propagation delay (using IDELAY) (HP I/O banks only) | 0.10 | 0.11 | 0.13 | 0.13 | ns |
| T_{IDIE3} | D pin to O pin propagation delay, no delay (HR I/O banks only) | 0.09 | 0.10 | 0.12 | 0.12 | ns |
| T_{IDIDE3} | DDL pin to O pin propagation delay (using IDELAY) (HR I/O banks only) | 0.10 | 0.11 | 0.13 | 0.13 | ns |
| Sequential Delays | | | | | | |
| T_{IDLOE2} | D pin to Q1 pin using flip-flop as a latch without delay (HP I/O banks only) | 0.36 | 0.39 | 0.45 | 0.45 | ns |
| T_{IDLDE2} | DDL pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only) | 0.36 | 0.39 | 0.45 | 0.45 | ns |
| T_{IDLOE3} | D pin to Q1 pin using flip-flop as a latch without delay (HR I/O banks only) | 0.36 | 0.39 | 0.45 | 0.45 | ns |
| T_{IDLDE3} | DDL pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only) | 0.36 | 0.39 | 0.45 | 0.45 | ns |
| T_{ICKQ} | CLK to Q outputs | 0.47 | 0.50 | 0.58 | 0.58 | ns |
| $T_{RQ_ILOGICE2}$ | SR pin to OQ/TQ out (HP I/O banks only) | 0.84 | 0.94 | 1.16 | 1.16 | ns |
| $T_{GSRQ_ILOGICE2}$ | Global set/reset to Q outputs (HP I/O banks only) | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| $T_{RQ_ILOGICE3}$ | SR pin to OQ/TQ out (HR I/O banks only) | 0.84 | 0.94 | 1.16 | 1.16 | ns |
| $T_{GSRQ_ILOGICE3}$ | Global set/reset to Q outputs (HR I/O banks only) | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| Set/Reset | | | | | | |
| $T_{RPW_ILOGICE2}$ | Minimum pulse width, SR inputs (HP I/O banks only) | 0.54 | 0.63 | 0.63 | 0.63 | ns, Min |
| $T_{RPW_ILOGICE3}$ | Minimum pulse width, SR inputs (HR I/O banks only) | 0.54 | 0.63 | 0.63 | 0.63 | ns, Min |

Table 25: OLOGIC Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--------------------------|--|-------------|------------|------------|------------|---------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Setup/Hold | | | | | | |
| T_{ODCK}/T_{OCKD} | D1/D2 pins setup/hold with respect to CLK | 0.45/-0.13 | 0.50/-0.13 | 0.58/-0.13 | 0.58/-0.13 | ns |
| T_{OOCECK}/T_{OCKOCE} | OCE pin setup/hold with respect to CLK | 0.28/0.03 | 0.29/0.03 | 0.45/0.03 | 0.45/0.03 | ns |
| T_{OSRCK}/T_{OCKSR} | SR pin setup/hold with respect to CLK | 0.32/0.18 | 0.38/0.18 | 0.70/0.18 | 0.70/0.18 | ns |
| T_{OTCK}/T_{OCKT} | T1/T2 pins setup/hold with respect to CLK | 0.49/-0.16 | 0.56/-0.16 | 0.68/-0.16 | 0.68/-0.13 | ns |
| T_{OTCECK}/T_{OCKTCE} | TCE pin setup/hold with respect to CLK | 0.28/0.01 | 0.30/0.01 | 0.45/0.01 | 0.45/0.06 | ns |
| Combinatorial | | | | | | |
| T_{ODQ} | D1 to OQ out or T1 to TQ out | 0.73 | 0.81 | 0.97 | 0.97 | ns |
| Sequential Delays | | | | | | |
| T_{OCKQ} | CLK to OQ/TQ out | 0.41 | 0.43 | 0.49 | 0.49 | ns |
| $T_{RQ_OLOGICE2}$ | SR pin to OQ/TQ out (HP I/O banks only) | 0.63 | 0.70 | 0.83 | 0.83 | ns |
| $T_{GSRQ_OLOGICE2}$ | Global set/reset to Q outputs (HP I/O banks only) | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| $T_{RQ_OLOGICE3}$ | SR pin to OQ/TQ out (HR I/O banks only) | 0.63 | 0.70 | 0.83 | 0.83 | ns |
| $T_{GSRQ_OLOGICE3}$ | Global set/reset to Q outputs (HR I/O banks only) | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| Set/Reset | | | | | | |
| $T_{RPW_OLOGICE2}$ | Minimum pulse width, SR inputs (HP I/O banks only) | 0.54 | 0.54 | 0.63 | 0.63 | ns, Min |
| $T_{RPW_OLOGICE3}$ | Minimum pulse width, SR inputs (HR I/O banks only) | 0.54 | 0.54 | 0.63 | 0.63 | ns, Min |

Input Serializer/Deserializer Switching Characteristics

Table 26: ISERDES Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|--|-------------|------------|------------|------------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Setup/Hold for Control Lines | | | | | | |
| $T_{ISCK_BITSLIP}/T_{ISCK_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV | 0.01/0.12 | 0.02/0.13 | 0.02/0.15 | 0.02/0.15 | ns |
| $T_{ISCK_CE} / T_{ISCK_CE}^{(2)}$ | CE pin setup/hold with respect to CLK (for CE1) | 0.39/-0.02 | 0.44/-0.02 | 0.63/-0.02 | 0.63/-0.02 | ns |
| $T_{ISCK_CE2} / T_{ISCK_CE2}^{(2)}$ | CE pin setup/hold with respect to CLKDIV (for CE2) | -0.12/0.29 | -0.12/0.31 | -0.12/0.35 | -0.12/0.35 | ns |
| Setup/Hold for Data Lines | | | | | | |
| T_{ISCK_D}/T_{ISCK_D} | D pin setup/hold with respect to CLK | -0.02/0.11 | -0.02/0.12 | -0.02/0.15 | -0.02/0.15 | ns |
| $T_{ISCK_DDL}/T_{ISCK_DDL}$ | DDL pin setup/hold with respect to CLK (using IDELAY) ⁽¹⁾ | -0.02/0.11 | -0.02/0.12 | -0.02/0.15 | -0.02/0.15 | ns |
| $T_{ISCK_D_DDR} / T_{ISCK_D_DDR}$ | D pin setup/hold with respect to CLK at DDR mode | -0.02/0.11 | -0.02/0.12 | -0.02/0.15 | -0.02/0.15 | ns |
| $T_{ISCK_DDL_DDR} / T_{ISCK_DDL_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾ | 0.11/0.11 | 0.12/0.12 | 0.15/0.15 | 0.15/0.15 | ns |
| Sequential Delays | | | | | | |
| T_{ISCK_Q} | CLKDIV to out at Q pin | 0.46 | 0.47 | 0.58 | 0.58 | ns |
| Propagation Delays | | | | | | |
| T_{ISDO_DO} | D input to DO output pin | 0.09 | 0.10 | 0.12 | 0.12 | ns |

Notes:

1. Recorded at 0 tap value.
2. T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 27: OSERDES Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------------------|---|-------------|------------|------------|------------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Setup/Hold | | | | | | |
| T_{OSDCK_D}/T_{OSCKD_D} | D input setup/hold with respect to CLKDIV | 0.37/0.02 | 0.40/0.02 | 0.55/0.02 | 0.55/0.02 | ns |
| $T_{OSDCK_T}/T_{OSCKD_T}^{(1)}$ | T input setup/hold with respect to CLK | 0.49/-0.15 | 0.56/-0.15 | 0.68/-0.15 | 0.68/-0.15 | ns |
| $T_{OSDCK_T2}/T_{OSCKD_T2}^{(1)}$ | T input setup/hold with respect to CLKDIV | 0.27/-0.15 | 0.30/-0.15 | 0.34/-0.15 | 0.34/-0.15 | ns |
| $T_{OSCK_OCE}/T_{OSCKC_OCE}$ | OCE input setup/hold with respect to CLK | 0.28/0.03 | 0.29/0.03 | 0.45/0.03 | 0.45/0.03 | ns |
| T_{OSCK_S} | SR (Reset) input setup with respect to CLKDIV | 0.41 | 0.46 | 0.75 | 0.75 | ns |
| $T_{OSCK_TCE}/T_{OSCKC_TCE}$ | TCE input setup/hold with respect to CLK | 0.28/0.01 | 0.30/0.01 | 0.45/0.01 | 0.45/0.01 | ns |
| Sequential Delays | | | | | | |
| T_{OSCKO_OQ} | Clock to out from CLK to OQ | 0.35 | 0.37 | 0.42 | 0.42 | ns |
| T_{OSCKO_TQ} | Clock to out from CLK to TQ | 0.41 | 0.43 | 0.49 | 0.49 | ns |
| Combinatorial | | | | | | |
| T_{OSDO_TTQ} | T input to TQ Out | 0.73 | 0.81 | 0.97 | 0.97 | ns |

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 28: Input/Output Delay Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|----------------------------------|------------|-----------|-----------|------------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| IDELAYCTRL | | | | | | |
| T_{DLYCCO_RDY} | Reset to ready for IDELAYCTRL | 3.22 | 3.22 | 3.22 | 3.22 | μ s |
| $F_{IDELAYCTRL_REF}$ | Attribute REFCLK frequency = 200.0 ⁽¹⁾ | 200 | 200 | 200 | 200 | MHz |
| | Attribute REFCLK frequency = 300.0 ⁽¹⁾ | 300 | 300 | N/A | N/A | MHz |
| | Attribute REFCLK frequency = 400.0 ⁽¹⁾ | 400 | 400 | N/A | N/A | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ± 10 | ± 10 | ± 10 | ± 10 | MHz |
| $T_{IDELAYCTRL_RPW}$ | Minimum reset pulse width | 52.00 | 52.00 | 52.00 | 52.00 | ns |
| IDELAY/ODELAY | | | | | | |
| $T_{IDELAYRESOLUTION}$ | IDELAY/ODELAY chain delay resolution | $1/(32 \times 2 \times F_{REF})$ | | | | μ s |
| $T_{IDELAYPAT_JIT}$ and $T_{ODELAYPAT_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾ | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾ | ± 5 | ± 5 | ± 5 | ± 5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾ | ± 9 | ± 9 | ± 9 | ± 9 | ps per tap |
| $T_{IDELAY_CLK_MAX}/$ $T_{ODELAY_CLK_MAX}$ | Maximum frequency of CLK input to IDELAY/ODELAY | 800 | 800 | 710 | 710 | MHz |
| $T_{IDCCK_CE}/ T_{IDCKC_CE}$ | CE pin setup/hold with respect to C for IDELAY | 0.11/0.10 | 0.14/0.12 | 0.18/0.14 | 0.18/0.14 | ns |
| $T_{ODCCK_CE}/ T_{ODCKC_CE}$ | CE pin setup/hold with respect to C for ODELAY | 0.14/0.03 | 0.16/0.04 | 0.19/0.05 | 0.19/0.05 | ns |
| $T_{IDCCK_INC}/ T_{IDCKC_INC}$ | INC pin setup/hold with respect to C for IDELAY | 0.10/0.14 | 0.12/0.16 | 0.14/0.20 | 0.14/0.20 | ns |
| $T_{ODCCK_INC}/ T_{ODCKC_INC}$ | INC pin setup/hold with respect to C for ODELAY | 0.10/0.07 | 0.12/0.08 | 0.13/0.09 | 0.13/0.09 | ns |
| $T_{IDCCK_RST}/ T_{IDCKC_RST}$ | RST pin setup/hold with respect to C for IDELAY | 0.13/0.08 | 0.14/0.10 | 0.16/0.12 | 0.16/0.12 | ns |
| $T_{ODCCK_RST}/ T_{ODCKC_RST}$ | RST pin setup/hold with respect to C for ODELAY | 0.16/0.04 | 0.19/0.06 | 0.24/0.08 | 0.24/0.08 | ns |
| $T_{IDDO_IDATAIN}$ | Propagation delay through IDELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| $T_{ODDO_ODATAIN}$ | Propagation delay through ODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 29: IO_FIFO Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|------------------------------------|------------------------|-------------|------------|------------|------------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| IO_FIFO Clock to Out Delays | | | | | | |
| T_{OFFCKO_DO} | RDCLK to Q outputs | 0.51 | 0.56 | 0.63 | 0.63 | ns |
| T_{CKO_FLAGS} | Clock to IO_FIFO flags | 0.59 | 0.62 | 0.81 | 0.81 | ns |
| Setup/Hold | | | | | | |
| T_{CCK_D}/T_{CKC_D} | D inputs to WRCLK | 0.43/-0.01 | 0.47/-0.01 | 0.53/-0.01 | 0.53/0.09 | ns |
| $T_{IFFCK_WREN}/T_{IFFCKC_WREN}$ | WREN to WRCLK | 0.39/-0.01 | 0.43/-0.01 | 0.50/-0.01 | 0.50/-0.01 | ns |
| $T_{OFFCK_RDEN}/T_{OFFCKC_RDEN}$ | RDEN to RDCLK | 0.49/0.01 | 0.53/0.02 | 0.61/0.02 | 0.61/0.02 | ns |
| Minimum Pulse Width | | | | | | |
| $T_{PWH_IO_FIFO}$ | RESET, RDCLK, WRCLK | 0.81 | 0.92 | 1.08 | 1.08 | ns |
| $T_{PWL_IO_FIFO}$ | RESET, RDCLK, WRCLK | 0.81 | 0.92 | 1.08 | 1.08 | ns |
| Maximum Frequency | | | | | | |
| F_{MAX} | RDCLK and WRCLK | 533.05 | 470.37 | 400.00 | 400.00 | MHz |

CLB Switching Characteristics

Table 30: CLB Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|--|-------------|------------|-----------|-----------|---------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Combinatorial Delays | | | | | | |
| T _{ILO} | An – Dn LUT address to A | 0.05 | 0.05 | 0.06 | 0.06 | ns, Max |
| T _{ILO_2} | An – Dn LUT address to AMUX/CMUX | 0.15 | 0.16 | 0.19 | 0.19 | ns, Max |
| T _{ILO_3} | An – Dn LUT address to BMUX_A | 0.24 | 0.25 | 0.30 | 0.30 | ns, Max |
| T _{ITO} | An – Dn inputs to A – D Q outputs | 0.58 | 0.61 | 0.74 | 0.74 | ns, Max |
| T _{AXA} | AX inputs to AMUX output | 0.38 | 0.40 | 0.49 | 0.49 | ns, Max |
| T _{AXB} | AX inputs to BMUX output | 0.40 | 0.42 | 0.52 | 0.52 | ns, Max |
| T _{AXC} | AX inputs to CMUX output | 0.39 | 0.41 | 0.50 | 0.50 | ns, Max |
| T _{AXD} | AX inputs to DMUX output | 0.43 | 0.44 | 0.52 | 0.52 | ns, Max |
| T _{BXB} | BX inputs to BMUX output | 0.31 | 0.33 | 0.40 | 0.40 | ns, Max |
| T _{BXD} | BX inputs to DMUX output | 0.38 | 0.39 | 0.47 | 0.47 | ns, Max |
| T _{CXC} | CX inputs to CMUX output | 0.27 | 0.28 | 0.34 | 0.34 | ns, Max |
| T _{CXD} | CX inputs to DMUX output | 0.33 | 0.34 | 0.41 | 0.41 | ns, Max |
| T _{DXD} | DX inputs to DMUX output | 0.32 | 0.33 | 0.40 | 0.40 | ns, Max |
| Sequential Delays | | | | | | |
| T _{CKO} | Clock to AQ – DQ outputs | 0.26 | 0.27 | 0.32 | 0.32 | ns, Max |
| T _{SHCKO} | Clock to AMUX – DMUX outputs | 0.32 | 0.32 | 0.39 | 0.39 | ns, Max |
| Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK | | | | | | |
| T _{AS} /T _{AH} | A _N – D _N input to CLK on A – D flip-flops | 0.01/0.12 | 0.02/0.13 | 0.03/0.18 | 0.03/0.24 | ns, Min |
| T _{DICK} /T _{CKDI} | A _X – D _X input to CLK on A – D flip-flops | 0.04/0.14 | 0.04/0.14 | 0.05/0.20 | 0.05/0.26 | ns, Min |
| | A _X – D _X input through MUXs and/or carry logic to CLK on A – D flip-flops | 0.36/0.10 | 0.37/0.11 | 0.46/0.16 | 0.46/0.22 | ns, Min |
| T _{CECK_CLB} /T _{CKCE_CLB} | CE input to CLK on A – D flip-flops | 0.19/0.05 | 0.20/0.05 | 0.25/0.05 | 0.25/0.11 | ns, Min |
| T _{SRCK} /T _{CKSR} | SR input to CLK on A – D flip-flops | 0.30/0.05 | 0.31/0.07 | 0.37/0.09 | 0.37/0.22 | ns, Min |
| Set/Reset | | | | | | |
| T _{SRMIN} | SR input minimum pulse width | 0.52 | 0.78 | 1.04 | 1.04 | ns, Min |
| T _{RQ} | Delay from SR input to AQ – DQ flip-flops | 0.38 | 0.38 | 0.46 | 0.46 | ns, Max |
| T _{CEO} | Delay from CE input to AQ – DQ flip-flops | 0.34 | 0.35 | 0.43 | 0.43 | ns, Max |
| F _{TOG} | Toggle frequency (for export control) | 1818 | 1818 | 1818 | 1818 | MHz |

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 31: CLB Distributed RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|---|-------------|------------|-----------|-----------|---------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Sequential Delays | | | | | | |
| $T_{SHCKO}^{(1)}$ | Clock to A – B outputs | 0.68 | 0.70 | 0.85 | 0.85 | ns, Max |
| T_{SHCKO_1} | Clock to AMUX – BMUX outputs | 0.91 | 0.95 | 1.15 | 1.15 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| $T_{DS_LDRAM}/T_{DH_LDRAM}$ | A – D inputs to CLK | 0.45/0.23 | 0.45/0.24 | 0.54/0.27 | 0.54/0.28 | ns, Min |
| $T_{AS_LDRAM}/T_{AH_LDRAM}$ | Address A inputs to clock | 0.13/0.50 | 0.14/0.50 | 0.17/0.58 | 0.17/0.61 | ns, Min |
| | Address A inputs through MUXs and/or carry logic to clock | 0.40/0.16 | 0.42/0.17 | 0.52/0.23 | 0.52/0.29 | ns, Min |
| $T_{WS_LDRAM}/T_{WH_LDRAM}$ | WE input to clock | 0.29/0.09 | 0.30/0.09 | 0.36/0.09 | 0.36/0.11 | ns, Min |
| $T_{CECK_LDRAM}/T_{CKCE_LDRAM}$ | CE input to CLK | 0.29/0.09 | 0.30/0.09 | 0.37/0.09 | 0.37/0.11 | ns, Min |
| Clock CLK | | | | | | |
| T_{MPW} | Minimum pulse width | 0.68 | 0.77 | 0.91 | 0.91 | ns, Min |
| T_{MCP} | Minimum clock period | 1.35 | 1.54 | 1.82 | 1.82 | ns, Min |

Notes:

- T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 32: CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|-------------------------------------|-------------|------------|-----------|-----------|---------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Sequential Delays | | | | | | |
| T_{REG} | Clock to A – D outputs | 0.96 | 0.98 | 1.20 | 1.20 | ns, Max |
| T_{REG_MUX} | Clock to AMUX – DMUX output | 1.19 | 1.23 | 1.50 | 1.50 | ns, Max |
| T_{REG_M31} | Clock to DMUX output via M31 output | 0.89 | 0.91 | 1.10 | 1.10 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| $T_{WS_SHFREG}/T_{WH_SHFREG}$ | WE input | 0.26/0.09 | 0.27/0.09 | 0.33/0.09 | 0.33/0.11 | ns, Min |
| $T_{CECK_SHFREG}/T_{CKCE_SHFREG}$ | CE input to CLK | 0.27/0.09 | 0.28/0.09 | 0.33/0.09 | 0.33/0.11 | ns, Min |
| $T_{DS_SHFREG}/T_{DH_SHFREG}$ | A – D inputs to CLK | 0.28/0.26 | 0.28/0.26 | 0.33/0.30 | 0.33/0.36 | ns, Min |
| Clock CLK | | | | | | |
| T_{MPW_SHFREG} | Minimum pulse width | 0.55 | 0.65 | 0.78 | 0.78 | ns, Min |

Block RAM and FIFO Switching Characteristics

Table 33: Block RAM and FIFO Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|---|-------------|------------|-----------|-----------|---------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Block RAM and FIFO Clock-to-Out Delays | | | | | | |
| T_{RCKO_DO} and $T_{RCKO_DO_REG}^{(1)}$ | Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾ | 1.57 | 1.80 | 2.08 | 2.08 | ns, Max |
| | Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾ | 0.54 | 0.63 | 0.75 | 0.75 | ns, Max |
| $T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$ | Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾ | 2.35 | 2.58 | 3.26 | 3.26 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾ | 0.62 | 0.69 | 0.80 | 0.80 | ns, Max |
| $T_{RCKO_DO_CASCOU}$ and $T_{RCKO_DO_CASCOU_REG}$ | Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾ | 2.21 | 2.45 | 2.80 | 2.80 | ns, Max |
| | Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾ | 0.98 | 1.08 | 1.24 | 1.24 | ns, Max |
| T_{RCKO_FLAGS} | Clock CLK to FIFO flags outputs ⁽⁶⁾ | 0.65 | 0.74 | 0.89 | 0.89 | ns, Max |
| $T_{RCKO_POINTERS}$ | Clock CLK to FIFO pointers outputs ⁽⁷⁾ | 0.79 | 0.87 | 0.98 | 0.98 | ns, Max |
| $T_{RCKO_PARITY_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.66 | 0.72 | 0.80 | 0.80 | ns, Max |
| $T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$ | Clock CLK to BITERR (without output register) | 2.17 | 2.38 | 3.01 | 3.01 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.57 | 0.65 | 0.76 | 0.76 | ns, Max |
| $T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.64 | 0.74 | 0.90 | 0.90 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.71 | 0.79 | 0.92 | 0.92 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| T_{RCKC_ADDR} / T_{RCKC_ADDR} | ADDR inputs ⁽⁸⁾ | 0.38/0.27 | 0.42/0.28 | 0.48/0.31 | 0.48/0.38 | ns, Min |
| $T_{RDCK_DI_WF_NC}$ / $T_{RCKD_DI_WF_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾ | 0.49/0.51 | 0.55/0.53 | 0.63/0.57 | 0.63/0.57 | ns, Min |
| $T_{RDCK_DI_RF}$ / $T_{RCKD_DI_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾ | 0.17/0.25 | 0.19/0.29 | 0.21/0.35 | 0.21/0.35 | ns, Min |
| $T_{RDCK_DI_ECC}$ / $T_{RCKD_DI_ECC}$ | DIN inputs with block RAM ECC in standard mode ⁽⁹⁾ | 0.42/0.37 | 0.47/0.39 | 0.53/0.43 | 0.53/0.58 | ns, Min |
| $T_{RDCK_DI_ECCW}$ / $T_{RCKD_DI_ECCW}$ | DIN inputs with block RAM ECC encode only ⁽⁹⁾ | 0.79/0.37 | 0.87/0.39 | 0.99/0.43 | 0.99/0.58 | ns, Min |
| $T_{RDCK_DI_ECC_FIFO}$ / $T_{RCKD_DI_ECC_FIFO}$ | DIN inputs with FIFO ECC in standard mode ⁽⁹⁾ | 0.89/0.47 | 0.98/0.50 | 1.12/0.54 | 1.12/0.69 | ns, Min |
| $T_{RCKC_INJECTBITERR}$ / $T_{RCKC_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.49/0.30 | 0.55/0.31 | 0.63/0.34 | 0.63/0.43 | ns, Min |
| T_{RCKC_EN} / T_{RCKC_EN} | Block RAM Enable (EN) input | 0.30/0.17 | 0.33/0.18 | 0.38/0.20 | 0.38/0.32 | ns, Min |
| T_{RCKC_REGCE} / T_{RCKC_REGCE} | CE input of output register | 0.21/0.13 | 0.25/0.13 | 0.31/0.14 | 0.31/0.19 | ns, Min |
| T_{RCKC_RSTREG} / T_{RCKC_RSTREG} | Synchronous RSTREG input | 0.25/0.06 | 0.27/0.06 | 0.29/0.06 | 0.29/0.14 | ns, Min |
| T_{RCKC_RSTRAM} / T_{RCKC_RSTRAM} | Synchronous RSTRAM input | 0.27/0.35 | 0.29/0.37 | 0.31/0.39 | 0.31/0.39 | ns, Min |
| T_{RCKC_WEA} / T_{RCKC_WEA} | Write Enable (WE) input (Block RAM only) | 0.38/0.15 | 0.41/0.16 | 0.46/0.17 | 0.46/0.29 | ns, Min |

Table 33: Block RAM and FIFO Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------------------|--|-------------|------------|------------|------------|---------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| $T_{RCKC_WREN}/T_{RCKC_WREN}$ | WREN FIFO inputs | 0.39/0.25 | 0.39/0.30 | 0.40/0.37 | 0.40/0.49 | ns, Min |
| $T_{RCKC_RDEN}/T_{RCKC_RDEN}$ | RDEN FIFO inputs | 0.36/0.26 | 0.36/0.30 | 0.37/0.37 | 0.37/0.49 | ns, Min |
| Reset Delays | | | | | | |
| T_{RCO_FLAGS} | Reset RST to FIFO flags/pointers ⁽¹⁰⁾ | 0.76 | 0.83 | 0.93 | 0.93 | ns, Max |
| $T_{RREC_RST}/T_{RREM_RST}$ | FIFO reset recovery and removal timing ⁽¹¹⁾ | 1.59/-0.68 | 1.76/-0.68 | 2.01/-0.68 | 2.01/-0.68 | ns, Max |
| Maximum Frequency | | | | | | |
| $F_{MAX_BRAM_WF_NC}$ | Block RAM (Write first and No change modes) When not in SDP RF mode | 601.32 | 543.77 | 458.09 | 458.09 | MHz |
| $F_{MAX_BRAM_RF_PERFORMANCE}$ | Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B | 601.32 | 543.77 | 458.09 | 458.09 | MHz |
| $F_{MAX_BRAM_RF_DELAYED_WRITE}$ | Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses | 528.26 | 477.33 | 400.80 | 400.80 | MHz |
| $F_{MAX_CAS_WF_NC}$ | Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode | 551.27 | 493.83 | 408.00 | 408.00 | MHz |
| $F_{MAX_CAS_RF_PERFORMANCE}$ | Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled | 551.27 | 493.83 | 408.00 | 408.00 | MHz |
| $F_{MAX_CAS_RF_DELAYED_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 478.24 | 427.35 | 350.88 | 350.88 | MHz |
| F_{MAX_FIFO} | FIFO in all modes without ECC | 601.32 | 543.77 | 458.09 | 458.09 | MHz |
| F_{MAX_ECC} | Block RAM and FIFO in ECC configuration | 484.26 | 430.85 | 351.12 | 351.12 | MHz |

Notes:

1. The timing report shows all of these parameters as T_{RCKO_DO} .
2. T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with $DO_REG = 0$.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
7. $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 34: DSP48E1 Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|-------------|------------|------------|------------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Setup and Hold Times of Data/Control Pins to the Input Register Clock | | | | | | |
| $T_{DSPDCK_A_AREG}/T_{DSPCKD_A_AREG}$ | A input to A register CLK | 0.24/0.12 | 0.27/0.14 | 0.31/0.16 | 0.33/0.18 | ns |
| $T_{DSPDCK_B_BREG}/T_{DSPCKD_B_BREG}$ | B input to B register CLK | 0.28/0.13 | 0.32/0.14 | 0.39/0.15 | 0.41/0.18 | ns |
| $T_{DSPDCK_C_CREG}/T_{DSPCKD_C_CREG}$ | C input to C register CLK | 0.15/0.15 | 0.17/0.17 | 0.20/0.20 | 0.20/0.22 | ns |
| $T_{DSPDCK_D_DREG}/T_{DSPCKD_D_DREG}$ | D input to D register CLK | 0.21/0.19 | 0.27/0.22 | 0.35/0.26 | 0.35/0.27 | ns |
| $T_{DSPDCK_ACIN_AREG}/T_{DSPCKD_ACIN_AREG}$ | ACIN input to A register CLK | 0.21/0.12 | 0.24/0.14 | 0.27/0.16 | 0.30/0.16 | ns |
| $T_{DSPDCK_BCIN_BREG}/T_{DSPCKD_BCIN_BREG}$ | BCIN input to B register CLK | 0.22/0.13 | 0.25/0.14 | 0.30/0.15 | 0.32/0.15 | ns |
| Setup and Hold Times of Data Pins to the Pipeline Register Clock | | | | | | |
| $T_{DSPDCK_A, B_MREG_MULT}/T_{DSPCKD_A, B_MREG_MULT}$ | {A, B} input to M register CLK using multiplier | 2.04/-0.01 | 2.34/-0.01 | 2.79/-0.01 | 2.79/-0.01 | ns |
| $T_{DSPDCK_A, D_ADREG}/T_{DSPCKD_A, D_ADREG}$ | {A, D} input to AD register CLK | 1.09/-0.02 | 1.25/-0.02 | 1.49/-0.02 | 1.49/-0.02 | ns |
| Setup and Hold Times of Data/Control Pins to the Output Register Clock | | | | | | |
| $T_{DSPDCK_A, B_PREG_MULT}/T_{DSPCKD_A, B_PREG_MULT}$ | {A, B,} input to P register CLK using multiplier | 3.41/-0.24 | 3.90/-0.24 | 4.64/-0.24 | 4.64/-0.24 | ns |
| $T_{DSPDCK_D_PREG_MULT}/T_{DSPCKD_D_PREG_MULT}$ | D input to P register CLK using multiplier | 3.33/-0.62 | 3.81/-0.62 | 4.53/-0.62 | 4.53/-0.62 | ns |
| $T_{DSPDCK_A, B_PREG}/T_{DSPCKD_A, B_PREG}$ | A or B input to P register CLK not using multiplier | 1.47/-0.24 | 1.68/-0.24 | 2.00/-0.24 | 2.00/-0.24 | ns |
| $T_{DSPDCK_C_PREG}/T_{DSPCKD_C_PREG}$ | C input to P register CLK not using multiplier | 1.30/-0.22 | 1.49/-0.22 | 1.78/-0.22 | 1.78/-0.22 | ns |
| $T_{DSPDCK_PCIN_PREG}/T_{DSPCKD_PCIN_PREG}$ | PCIN input to P register CLK | 1.12/-0.13 | 1.28/-0.13 | 1.52/-0.13 | 1.52/-0.13 | ns |
| Setup and Hold Times of the CE Pins | | | | | | |
| $T_{DSPDCK_CEA, CEB_AREG, BREG}/T_{DSPCKD_CEA, CEB_AREG, BREG}$ | {CEA, CEB} input to {A, B} register CLK | 0.30/0.05 | 0.36/0.06 | 0.44/0.09 | 0.44/0.09 | ns |
| $T_{DSPDCK_CEC_CREG}/T_{DSPCKD_CEC_CREG}$ | CEC input to C register CLK | 0.24/0.08 | 0.29/0.09 | 0.36/0.11 | 0.36/0.11 | ns |
| $T_{DSPDCK_CED_DREG}/T_{DSPCKD_CED_DREG}$ | CED input to D register CLK | 0.31/-0.02 | 0.36/-0.02 | 0.44/-0.02 | 0.44/0.02 | ns |
| $T_{DSPDCK_CEM_MREG}/T_{DSPCKD_CEM_MREG}$ | CEM input to M register CLK | 0.26/0.15 | 0.29/0.17 | 0.33/0.20 | 0.33/0.20 | ns |
| $T_{DSPDCK_CEP_PREG}/T_{DSPCKD_CEP_PREG}$ | CEP input to P register CLK | 0.31/0.01 | 0.36/0.01 | 0.45/0.01 | 0.45/0.01 | ns |
| Setup and Hold Times of the RST Pins | | | | | | |
| $T_{DSPDCK_RSTA, RSTB_AREG, BREG}/T_{DSPCKD_RSTA, RSTB_AREG, BREG}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.34/0.10 | 0.39/0.11 | 0.47/0.13 | 0.47/0.14 | ns |
| $T_{DSPDCK_RSTC_CREG}/T_{DSPCKD_RSTC_CREG}$ | RSTC input to C register CLK | 0.06/0.22 | 0.07/0.24 | 0.08/0.26 | 0.08/0.26 | ns |
| $T_{DSPDCK_RSTD_DREG}/T_{DSPCKD_RSTD_DREG}$ | RSTD input to D register CLK | 0.37/0.06 | 0.42/0.06 | 0.50/0.07 | 0.50/0.07 | ns |
| $T_{DSPDCK_RSTM_MREG}/T_{DSPCKD_RSTM_MREG}$ | RSTM input to M register CLK | 0.18/0.18 | 0.20/0.21 | 0.23/0.24 | 0.23/0.24 | ns |
| $T_{DSPDCK_RSTP_PREG}/T_{DSPCKD_RSTP_PREG}$ | RSTP input to P register CLK | 0.24/0.01 | 0.26/0.01 | 0.30/0.01 | 0.30/0.11 | ns |
| Combinatorial Delays from Input Pins to Output Pins | | | | | | |
| $T_{DSPDO_A_CARRYOUT_MULT}$ | A input to CARRYOUT output using multiplier | 3.21 | 3.69 | 4.39 | 4.39 | ns |
| $T_{DSPDO_D_P_MULT}$ | D input to P output using multiplier | 3.15 | 3.61 | 4.30 | 4.30 | ns |

Table 34: DSP48E1 Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|--|--|-------------|------------|------|------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| T _{DSPDO_A_P} | A input to P output not using multiplier | 1.30 | 1.48 | 1.76 | 1.76 | ns |
| T _{DSPDO_C_P} | C input to P output | 1.13 | 1.30 | 1.55 | 1.55 | ns |
| Combinatorial Delays from Input Pins to Cascading Output Pins | | | | | | |
| T _{DSPDO_{A; B}_{ACOUT; BCOUT}} | {A, B} input to {ACOUT, BCOUT} output | 0.47 | 0.53 | 0.63 | 0.63 | ns |
| T _{DSPDO_{A, B}_CARRYCASCOUT_MULT} | {A, B} input to CARRYCASCOUT output using multiplier | 3.44 | 3.94 | 4.69 | 4.69 | ns |
| T _{DSPDO_D_CARRYCASCOUT_MULT} | D input to CARRYCASCOUT output using multiplier | 3.36 | 3.85 | 4.58 | 4.58 | ns |
| T _{DSPDO_{A, B}_CARRYCASCOUT} | {A, B} input to CARRYCASCOUT output not using multiplier | 1.50 | 1.72 | 2.04 | 2.04 | ns |
| T _{DSPDO_C_CARRYCASCOUT} | C input to CARRYCASCOUT output | 1.34 | 1.53 | 1.83 | 1.83 | ns |
| Combinatorial Delays from Cascading Input Pins to All Output Pins | | | | | | |
| T _{DSPDO_ACIN_P_MULT} | ACIN input to P output using multiplier | 3.09 | 3.55 | 4.24 | 4.24 | ns |
| T _{DSPDO_ACIN_P} | ACIN input to P output not using multiplier | 1.16 | 1.33 | 1.59 | 1.59 | ns |
| T _{DSPDO_ACIN_ACOUT} | ACIN input to ACOUT output | 0.32 | 0.37 | 0.45 | 0.45 | ns |
| T _{DSPDO_ACIN_CARRYCASCOUT_MULT} | ACIN input to CARRYCASCOUT output using multiplier | 3.30 | 3.79 | 4.52 | 4.52 | ns |
| T _{DSPDO_ACIN_CARRYCASCOUT} | ACIN input to CARRYCASCOUT output not using multiplier | 1.37 | 1.57 | 1.87 | 1.87 | ns |
| T _{DSPDO_PCIN_P} | PCIN input to P output | 0.94 | 1.08 | 1.29 | 1.29 | ns |
| T _{DSPDO_PCIN_CARRYCASCOUT} | PCIN input to CARRYCASCOUT output | 1.15 | 1.32 | 1.57 | 1.57 | ns |
| Clock to Outs from Output Register Clock to Output Pins | | | | | | |
| T _{DSPCKO_P_PREG} | CLK PREG to P output | 0.33 | 0.35 | 0.39 | 0.39 | ns |
| T _{DSPCKO_CARRYCASCOUT_PREG} | CLK PREG to CARRYCASCOUT output | 0.44 | 0.50 | 0.59 | 0.59 | ns |
| Clock to Outs from Pipeline Register Clock to Output Pins | | | | | | |
| T _{DSPCKO_P_MREG} | CLK MREG to P output | 1.42 | 1.64 | 1.96 | 1.96 | ns |
| T _{DSPCKO_CARRYCASCOUT_MREG} | CLK MREG to CARRYCASCOUT output | 1.63 | 1.87 | 2.24 | 2.24 | ns |
| T _{DSPCKO_P_ADREG_MULT} | CLK ADREG to P output using multiplier | 2.30 | 2.63 | 3.13 | 3.13 | ns |
| T _{DSPCKO_CARRYCASCOUT_ADREG_MULT} | CLK ADREG to CARRYCASCOUT output using multiplier | 2.51 | 2.87 | 3.41 | 3.41 | ns |

Table 34: DSP48E1 Switching Characteristics (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|---|--|-------------|------------|--------|--------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Clock to Outs from Input Register Clock to Output Pins | | | | | | |
| $T_{\text{DSPCKO_P_AREG_MULT}}$ | CLK AREG to P output using multiplier | 3.34 | 3.83 | 4.55 | 4.55 | ns |
| $T_{\text{DSPCKO_P_BREG}}$ | CLK BREG to P output not using multiplier | 1.39 | 1.59 | 1.88 | 1.88 | ns |
| $T_{\text{DSPCKO_P_CREG}}$ | CLK CREG to P output not using multiplier | 1.43 | 1.64 | 1.95 | 1.95 | ns |
| $T_{\text{DSPCKO_P_DREG_MULT}}$ | CLK DREG to P output using multiplier | 3.32 | 3.80 | 4.51 | 4.51 | ns |
| Clock to Outs from Input Register Clock to Cascading Output Pins | | | | | | |
| $T_{\text{DSPCKO_}\{ACOUT; BCOUT\}_}\{AREG; BREG\}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.55 | 0.62 | 0.74 | 0.74 | ns |
| $T_{\text{DSPCKO_CARRYCASCOUT_}\{AREG, BREG\}_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 3.55 | 4.06 | 4.84 | 4.84 | ns |
| $T_{\text{DSPCKO_CARRYCASCOUT_BREG}}$ | CLK (BREG) to CARRYCASCOUT output not using multiplier | 1.60 | 1.82 | 2.16 | 2.16 | ns |
| $T_{\text{DSPCKO_CARRYCASCOUT_DREG_MULT}}$ | CLK (DREG) to CARRYCASCOUT output using multiplier | 3.52 | 4.03 | 4.79 | 4.79 | ns |
| $T_{\text{DSPCKO_CARRYCASCOUT_CREG}}$ | CLK (CREG) to CARRYCASCOUT output | 1.64 | 1.88 | 2.23 | 2.23 | ns |
| Maximum Frequency | | | | | | |
| F_{MAX} | With all registers used | 741.84 | 650.20 | 547.95 | 547.95 | MHz |
| $F_{\text{MAX_PATDET}}$ | With pattern detector | 627.35 | 549.75 | 463.61 | 463.61 | MHz |
| $F_{\text{MAX_MULT_NOMREG}}$ | Two register multiply without MREG | 412.20 | 360.75 | 303.77 | 303.77 | MHz |
| $F_{\text{MAX_MULT_NOMREG_PATDET}}$ | Two register multiply without MREG with pattern detect | 374.25 | 327.65 | 276.01 | 276.01 | MHz |
| $F_{\text{MAX_PREADD_MULT_NOADREG}}$ | Without ADREG | 468.82 | 408.66 | 342.70 | 342.70 | MHz |
| $F_{\text{MAX_PREADD_MULT_NOADREG_PATDET}}$ | Without ADREG with pattern detect | 468.82 | 408.66 | 342.70 | 342.70 | MHz |
| $F_{\text{MAX_NOPIPELINEREG}}$ | Without pipeline registers (MREG, ADREG) | 306.84 | 267.81 | 225.02 | 225.02 | MHz |
| $F_{\text{MAX_NOPIPELINEREG_PATDET}}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 285.23 | 249.13 | 209.38 | 209.38 | MHz |

Clock Buffers and Networks

Table 35: Global Clock Switching Characteristics (Including BUFGCTRL)

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------------------|--------------------------------|-------------|------------|-----------|-----------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| $T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$ | CE pins setup/hold | 0.12/0.30 | 0.14/0.38 | 0.26/0.38 | 0.26/0.92 | ns |
| $T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$ | S pins setup/hold | 0.12/0.30 | 0.14/0.38 | 0.26/0.38 | 0.26/0.92 | ns |
| $T_{BCKKO_O}^{(2)}$ | BUFGCTRL delay from I0/I1 to O | 0.08 | 0.10 | 0.12 | 0.12 | ns |
| Maximum Frequency | | | | | | |
| F_{MAX_BUFG} | Global clock tree (BUFG) | 741.00 | 710.00 | 625.00 | 625.00 | MHz |

Notes:

- T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
- T_{BCKKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKKO_O} values.

Table 36: Input/Output Clock Switching Characteristics (BUFIO)

| Symbol | Description | Speed Grade | | | | Units |
|--------------------------|--------------------------------|-------------|------------|--------|--------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| T_{BIOCKO_O} | Clock to out delay from I to O | 1.04 | 1.14 | 1.32 | 1.32 | ns |
| Maximum Frequency | | | | | | |
| F_{MAX_BUFIO} | I/O clock tree (BUFIO) | 800.00 | 800.00 | 710.00 | 710.00 | MHz |

Table 37: Regional Clock Buffer Switching Characteristics (BUFR)

| Symbol | Description | Speed Grade | | | | Units |
|--------------------------|---|-------------|------------|--------|--------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| T_{BRCKO_O} | Clock to out delay from I to O | 0.60 | 0.65 | 0.77 | 0.77 | ns |
| $T_{BRCKO_O_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set | 0.30 | 0.32 | 0.38 | 0.38 | ns |
| T_{BRDO_O} | Propagation delay from CLR to O | 0.71 | 0.75 | 0.96 | 0.96 | ns |
| Maximum Frequency | | | | | | |
| $F_{MAX_BUFR}^{(1)}$ | Regional clock tree (BUFR) | 600.00 | 540.00 | 450.00 | 450.00 | MHz |

Notes:

- The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 38: Horizontal Clock Buffer Switching Characteristics (BUFH)

| Symbol | Description | Speed Grade | | | | Units |
|-----------------------------|--------------------------------|-------------|------------|-----------|-----------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| T_{BHCKO_O} | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.13 | ns |
| T_{BHCK_CE}/T_{BHCK_CE} | CE pin setup and hold | 0.20/0.16 | 0.23/0.20 | 0.38/0.21 | 0.38/0.79 | ns |
| Maximum Frequency | | | | | | |
| F_{MAX_BUFH} | Horizontal clock buffer (BUFH) | 741.00 | 710.00 | 625.00 | 625.00 | MHz |

Table 39: Duty Cycle Distortion and Clock Tree Skew

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|------------------------|--|------------|-------------|------|------|------|------|------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| T _{DCD_CLK} | Global clock tree duty cycle distortion ⁽¹⁾ | All | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| T _{CKSKEW} | Global clock tree skew ⁽²⁾ | XC7V585T | 0.75 | N/A | 0.91 | 0.91 | 0.98 | N/A | ns |
| | | XC7V2000T | N/A | 0.39 | 0.39 | 0.39 | 0.39 | N/A | ns |
| | | XC7VX330T | 0.60 | N/A | 0.74 | 0.74 | 0.79 | N/A | ns |
| | | XC7VX415T | 0.76 | N/A | 0.84 | 0.84 | 0.91 | N/A | ns |
| | | XC7VX485T | 0.60 | N/A | 0.74 | 0.74 | 0.79 | N/A | ns |
| | | XC7VX550T | 0.73 | N/A | 0.88 | 0.88 | 0.96 | N/A | ns |
| | | XC7VX690T | 0.73 | N/A | 0.88 | 0.88 | 0.96 | N/A | ns |
| | | XC7VX980T | N/A | N/A | 0.91 | 0.91 | 0.98 | N/A | ns |
| | | XC7VX1140T | N/A | 0.39 | 0.39 | 0.39 | 0.39 | N/A | ns |
| | | XQ7V585T | N/A | N/A | 0.91 | 0.91 | 0.98 | 0.98 | ns |
| | | XQ7VX330T | N/A | N/A | 0.74 | 0.74 | 0.79 | 0.79 | ns |
| | | XQ7VX485T | N/A | N/A | 0.74 | 0.74 | 0.79 | 0.79 | ns |
| | | XQ7VX690T | N/A | N/A | 0.88 | N/A | 0.96 | N/A | ns |
| XQ7VX980T | N/A | N/A | N/A | 0.91 | 0.98 | N/A | ns | | |
| T _{DCD_BUFIO} | I/O clock tree duty cycle distortion | All | 0.12 | 0.12 | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| T _{BUFIOSKEW} | I/O clock tree skew across one clock region | All | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | ns |
| T _{DCD_BUFR} | Regional clock tree duty cycle distortion | All | 0.15 | 0.15 | 0.15 | 0.15 | 0.15 | 0.15 | ns |

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 40: MMCM Specification

| Symbol | Description | Speed Grade | | | | Units |
|-----------------------------|---|---|------------|---------|---------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| MMCM_F _{INMAX} | Maximum input clock frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| MMCM_F _{INMIN} | Minimum input clock frequency | 10 | 10 | 10 | 10 | MHz |
| MMCM_F _{INJITTER} | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_F _{INDUTY} | Allowable input duty cycle: 10—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| MMCM_F _{MIN_PSCLK} | Minimum dynamic phase shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| MMCM_F _{MAX_PSCLK} | Maximum dynamic phase shift clock frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_F _{VCOMIN} | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| MMCM_F _{VCOMAX} | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |

Table 40: MMCM Specification (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|--|--|---|------------|-----------|-----------|----------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| MMCM_F _{BANDWIDTH} | Low MMCM bandwidth at typical ⁽¹⁾ | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical ⁽¹⁾ | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| MMCM_T _{STATPHAOFFSET} | Static phase offset of the MMCM outputs ⁽²⁾ | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| MMCM_T _{OUTJITTER} | MMCM output jitter | Note 3 | | | | |
| MMCM_T _{OUTDUTY} | MMCM output clock duty cycle precision ⁽⁴⁾ | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| MMCM_T _{LOCKMAX} | MMCM maximum Lock Time | 100 | 100 | 100 | 100 | µs |
| MMCM_F _{OUTMAX} | MMCM maximum output frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| MMCM_F _{OUTMIN} | MMCM minimum output frequency ⁽⁵⁾⁽⁶⁾ | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| MMCM_T _{EXTFDVAR} | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_RST _{MINPULSE} | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_F _{PFDMAX} | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| MMCM_F _{PFDMIN} | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_T _{FBDelay} | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| MMCM Switching Characteristics Setup and Hold | | | | | | |
| T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN} | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC} | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| T _{MMCMCKO_PSDONE} | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.81 | ns |
| Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK | | | | | | |
| T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR} | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| T _{MMCMDCK_DI} / T _{MMCMCKD_DI} | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| T _{MMCMDCK_DEN} / T _{MMCMCKD_DEN} | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| T _{MMCMDCK_DWE} / T _{MMCMCKD_DWE} | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| T _{MMCMCKO_DRDY} | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| F _{DCK} | DCLK frequency | 200.00 | 200.00 | 200.00 | 200.00 | MHz, Max |

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 41: PLL Specification

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|------------|-----------|-----------|----------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| PLL_F _{INMAX} | Maximum input clock frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| PLL_F _{INMIN} | Minimum input clock frequency | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_F _{INJITTER} | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | |
| PLL_F _{INDUTY} | Allowable input duty cycle: 19—49 MHz | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | % |
| PLL_F _{VCOMIN} | Minimum PLL VCO frequency | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_F _{VCOMAX} | Maximum PLL VCO frequency | 2133.00 | 1866.00 | 1600.00 | 1600.00 | MHz |
| PLL_F _{BANDWIDTH} | Low PLL bandwidth at typical ⁽¹⁾ | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical ⁽¹⁾ | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| PLL_T _{STATPHAOFFSET} | Static phase offset of the PLL outputs ⁽²⁾ | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| PLL_T _{OUTJITTER} | PLL output jitter | Note 3 | | | | |
| PLL_T _{OUTDUTY} | PLL output clock duty cycle precision ⁽⁴⁾ | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| PLL_T _{LOCKMAX} | PLL maximum lock time | 100 | 100 | 100 | 100 | μs |
| PLL_F _{OUTMAX} | PLL maximum output frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| PLL_F _{OUTMIN} | PLL minimum output frequency ⁽⁵⁾ | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| PLL_T _{EXTFDVAR} | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | |
| PLL_RST _{MINPULSE} | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| PLL_F _{PFDMAX} | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| PLL_F _{PFDMIN} | Minimum frequency at the phase frequency detector | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_T _{FBDELAY} | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | |
| Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK | | | | | | |
| T _{PLLDCK_DADDR} / T _{PLLCDK_DADDR} | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| T _{PLLDCK_DI} / T _{PLLCDK_DI} | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| T _{PLLDCK_DEN} / T _{PLLCDK_DEN} | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| T _{PLLDCK_DWE} / T _{PLLCDK_DWE} | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| T _{PLLDCKO_DRDY} | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | ns, Max |
| F _{DCK} | DCLK frequency | 200.00 | 200.00 | 200.00 | 200.00 | MHz, Max |

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 42: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)⁽¹⁾

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|------------|-------------|------|------|------|------|------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL. | | | | | | | | | |
| T _{TICKOFF} | Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs <i>without</i> MMCM/PLL (near clock region) ⁽²⁾ | XC7V585T | 5.63 | N/A | 6.20 | 6.20 | 6.97 | N/A | ns |
| | | XC7V2000T | N/A | 5.66 | 5.66 | 5.66 | 6.35 | N/A | ns |
| | | XC7VX330T | 5.41 | N/A | 5.97 | 5.97 | 6.71 | N/A | ns |
| | | XC7VX415T | 5.46 | N/A | 5.96 | 5.96 | 6.70 | N/A | ns |
| | | XC7VX485T | 5.29 | N/A | 5.84 | 5.84 | 6.57 | N/A | ns |
| | | XC7VX550T | 5.45 | N/A | 6.02 | 6.02 | 6.76 | N/A | ns |
| | | XC7VX690T | 5.46 | N/A | 6.02 | 6.02 | 6.76 | N/A | ns |
| | | XC7VX980T | N/A | N/A | 6.12 | 6.12 | 6.87 | N/A | ns |
| | | XC7VX1140T | N/A | 5.59 | 5.59 | 5.59 | 6.28 | N/A | ns |
| | | XQ7V585T | N/A | N/A | 6.20 | 6.20 | 6.97 | 6.97 | ns |
| | | XQ7VX330T | N/A | N/A | 5.97 | 5.97 | 6.71 | 6.71 | ns |
| | | XQ7VX485T | N/A | N/A | 5.84 | 5.84 | 6.57 | 6.57 | ns |
| | | XQ7VX690T | N/A | N/A | 6.02 | N/A | 6.76 | N/A | ns |
| XQ7VX980T | N/A | N/A | N/A | 6.12 | 6.87 | N/A | ns | | |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
2. Refer to the Die Level Bank Numbering Overview section of *7 Series FPGA Packaging and Pinout Specification* ([UG475](#)).

Table 43: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)⁽¹⁾

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|------------|-------------|------|------|------|------|------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL. | | | | | | | | | |
| T _{ICKOFFAR} | Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs <i>without</i> MMCM/PLL (far clock region) ⁽²⁾ | XC7V585T | 6.81 | N/A | 7.53 | 7.53 | 8.44 | N/A | ns |
| | | XC7V2000T | N/A | 6.00 | 6.00 | 6.00 | 6.73 | N/A | ns |
| | | XC7VX330T | 6.31 | N/A | 6.97 | 6.97 | 7.83 | N/A | ns |
| | | XC7VX415T | 6.36 | N/A | 6.90 | 6.90 | 7.69 | N/A | ns |
| | | XC7VX485T | 6.20 | N/A | 6.86 | 6.86 | 7.69 | N/A | ns |
| | | XC7VX550T | 6.66 | N/A | 7.37 | 7.37 | 8.27 | N/A | ns |
| | | XC7VX690T | 6.69 | N/A | 7.37 | 7.37 | 8.27 | N/A | ns |
| | | XC7VX980T | N/A | N/A | 7.47 | 7.47 | 8.37 | N/A | ns |
| | | XC7VX1140T | N/A | 5.93 | 5.93 | 5.93 | 6.65 | N/A | ns |
| | | XQ7V585T | N/A | N/A | 7.53 | 7.53 | 8.44 | 8.44 | ns |
| | | XQ7VX330T | N/A | N/A | 6.97 | 6.97 | 7.83 | 7.83 | ns |
| | | XQ7VX485T | N/A | N/A | 6.86 | 6.86 | 7.69 | 7.69 | ns |
| | | XQ7VX690T | N/A | N/A | 7.37 | N/A | 8.27 | N/A | ns |
| | | XQ7VX980T | N/A | N/A | N/A | 7.47 | 8.37 | N/A | ns |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
2. Refer to the Die Level Bank Numbering Overview section of *7 Series FPGA Packaging and Pinout Specification* ([UG475](#)).

Table 44: Clock-Capable Clock Input to Output Delay With MMCM

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|--|--|------------|-------------|------|------|------|------|------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM. | | | | | | | | | |
| T _{ICKOFMMCMCC} | Clock-capable clock input and OUTFF <i>with</i> MMCM | XC7V585T | 1.07 | N/A | 1.07 | 1.07 | 1.07 | N/A | ns |
| | | XC7V2000T | N/A | 0.82 | 0.82 | 0.82 | 0.82 | N/A | ns |
| | | XC7VX330T | 1.01 | N/A | 1.01 | 1.01 | 1.01 | N/A | ns |
| | | XC7VX415T | 1.07 | N/A | 1.07 | 1.07 | 1.07 | N/A | ns |
| | | XC7VX485T | 0.91 | N/A | 0.91 | 0.91 | 0.91 | N/A | ns |
| | | XC7VX550T | 0.97 | N/A | 0.97 | 0.97 | 0.97 | N/A | ns |
| | | XC7VX690T | 1.07 | N/A | 1.07 | 1.07 | 1.07 | N/A | ns |
| | | XC7VX980T | N/A | N/A | 0.96 | 0.96 | 0.96 | N/A | ns |
| | | XC7VX1140T | N/A | 0.82 | 0.82 | 0.82 | 0.82 | N/A | ns |
| | | XQ7V585T | N/A | N/A | 1.07 | 1.07 | 1.07 | 1.07 | ns |
| | | XQ7VX330T | N/A | N/A | 1.01 | 1.01 | 1.01 | 1.01 | ns |
| | | XQ7VX485T | N/A | N/A | 0.91 | 0.91 | 0.91 | 0.91 | ns |
| | | XQ7VX690T | N/A | N/A | 1.07 | N/A | 1.07 | N/A | ns |
| | | XQ7VX980T | N/A | N/A | N/A | 0.96 | 0.96 | N/A | ns |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Table 45: Clock-Capable Clock Input to Output Delay With PLL

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|------------|-------------|------|------|------|------|------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL. | | | | | | | | | |
| T _{ICKOFFLLCC} | Clock-capable clock input and OUTFF <i>with</i> PLL | XC7V585T | 0.96 | N/A | 0.96 | 0.96 | 0.96 | N/A | ns |
| | | XC7V2000T | N/A | 0.71 | 0.71 | 0.71 | 0.71 | N/A | ns |
| | | XC7VX330T | 0.90 | N/A | 0.90 | 0.90 | 0.90 | N/A | ns |
| | | XC7VX415T | 0.96 | N/A | 0.96 | 0.96 | 0.96 | N/A | ns |
| | | XC7VX485T | 0.80 | N/A | 0.80 | 0.80 | 0.80 | N/A | ns |
| | | XC7VX550T | 0.86 | N/A | 0.86 | 0.86 | 0.86 | N/A | ns |
| | | XC7VX690T | 0.96 | N/A | 0.96 | 0.96 | 0.96 | N/A | ns |
| | | XC7VX980T | N/A | N/A | 0.85 | 0.85 | 0.85 | N/A | ns |
| | | XC7VX1140T | N/A | 0.71 | 0.71 | 0.71 | 0.71 | N/A | ns |
| | | XQ7V585T | N/A | N/A | 0.96 | 0.96 | 0.96 | 0.96 | ns |
| | | XQ7VX330T | N/A | N/A | 0.90 | 0.90 | 0.90 | 0.90 | ns |
| | | XQ7VX485T | N/A | N/A | 0.80 | 0.80 | 0.80 | 0.80 | ns |
| | | XQ7VX690T | N/A | N/A | 0.96 | N/A | 0.96 | N/A | ns |
| | | XQ7VX980T | N/A | N/A | N/A | 0.85 | 0.85 | N/A | ns |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
2. PLL output jitter is already included in the timing calculation.

Table 46: Pin-to-Pin, Clock-to-Out using BUFIO

| Symbol | Description | Speed Grade | | | | Units |
|---|--|-------------|------------|------|------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> BUFIO. | | | | | | |
| T _{ICKOFFCS} | Clock-to-out of I/O clock for HR I/O banks | 4.93 | 5.52 | 6.20 | 6.20 | ns |
| | Clock-to-out of I/O clock for HP I/O banks | 4.85 | 5.44 | 6.11 | 6.11 | ns |

Device Pin-to-Pin Input Parameter Guidelines

Table 47: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks (only)

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|--|------------|-------------|-----|------------|------------|------------|------------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾ | | | | | | | | | |
| T _{PSFD} /T _{PHFD} | Full delay (legacy delay or default delay) Global clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7V585T | 3.12/-0.37 | N/A | 3.19/-0.37 | 3.19/-0.37 | 3.42/-0.37 | N/A | ns |
| | | XC7V2000T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XC7VX330T | 2.90/-0.31 | N/A | 2.96/-0.31 | 2.96/-0.31 | 3.16/-0.31 | N/A | ns |
| | | XC7VX415T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XC7VX485T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XC7VX550T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XC7VX690T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XC7VX980T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XC7VX1140T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XQ7V585T | N/A | N/A | 3.19/-0.37 | 3.19/-0.37 | 3.42/-0.37 | 3.42/-0.37 | ns |
| | | XQ7VX330T | N/A | N/A | 2.96/-0.31 | 2.96/-0.31 | 3.16/-0.31 | 3.16/-0.31 | ns |
| | | XQ7VX485T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XQ7VX690T | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| | | XQ7VX980T | N/A | N/A | N/A | N/A | N/A | N/A | ns |

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch

Table 48: Clock-Capable Clock Input Setup and Hold With MMCM

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|--|---|------------|-------------|------------|------------|------------|------------|------------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾ | | | | | | | | | |
| T _{PSMMCMCC} / T _{PHMMCMCC} | No delay clock-capable clock input and IFF ⁽³⁾ with MMCM | XC7V585T | 2.71/-0.10 | N/A | 3.00/-0.10 | 3.00/-0.10 | 3.33/-0.10 | N/A | ns |
| | | XC7V2000T | N/A | 2.60/-0.24 | 2.60/-0.24 | 2.60/-0.24 | 2.87/-0.24 | N/A | ns |
| | | XC7VX330T | 2.58/-0.15 | N/A | 2.87/-0.15 | 2.87/-0.15 | 3.18/-0.15 | N/A | ns |
| | | XC7VX415T | 2.73/0.01 | N/A | 3.03/0.01 | 3.03/0.01 | 3.36/0.01 | N/A | ns |
| | | XC7VX485T | 2.58/-0.15 | N/A | 2.87/-0.15 | 2.87/-0.15 | 3.18/-0.15 | N/A | ns |
| | | XC7VX550T | 2.72/-0.09 | N/A | 3.01/-0.09 | 3.01/-0.09 | 3.34/-0.09 | N/A | ns |
| | | XC7VX690T | 2.72/0.01 | N/A | 3.01/0.01 | 3.01/0.01 | 3.34/0.01 | N/A | ns |
| | | XC7VX980T | N/A | N/A | 3.00/-0.10 | 3.00/-0.10 | 3.33/-0.10 | N/A | ns |
| | | XC7VX1140T | N/A | 2.61/-0.24 | 2.61/-0.24 | 2.61/-0.24 | 2.88/-0.24 | N/A | ns |
| | | XQ7V585T | N/A | N/A | 3.00/-0.10 | 3.00/-0.10 | 3.33/-0.10 | 3.33/-0.10 | ns |
| | | XQ7VX330T | N/A | N/A | 2.87/-0.15 | 2.87/-0.15 | 3.18/-0.15 | 3.18/-0.15 | ns |
| | | XQ7VX485T | N/A | N/A | 2.87/-0.15 | 2.87/-0.15 | 3.18/-0.15 | 3.18/-0.15 | ns |
| | | XQ7VX690T | N/A | N/A | 3.01/0.01 | N/A | 3.34/0.01 | N/A | ns |
| | | XQ7VX980T | N/A | N/A | N/A | 3.00/-0.10 | 3.33/-0.10 | N/A | ns |

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 49: Clock-Capable Clock Input Setup and Hold With PLL

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|--|------------|-------------|------------|------------|------------|------------|------------|-------|
| | | | -3 | -2G | -2 | -2L | -1 | -1M | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾ | | | | | | | | | |
| T _{PSPLLCC} / T _{PHPLLCC} | No delay clock-capable clock input and IFF ⁽³⁾ with PLL | XC7V585T | 3.07/-0.21 | N/A | 3.40/-0.21 | 3.40/-0.21 | 3.72/-0.21 | N/A | ns |
| | | XC7V2000T | N/A | 2.99/-0.35 | 2.99/-0.35 | 2.99/-0.35 | 3.27/-0.35 | N/A | ns |
| | | XC7VX330T | 2.94/-0.26 | N/A | 3.26/-0.26 | 3.26/-0.26 | 3.57/-0.26 | N/A | ns |
| | | XC7VX415T | 3.09/-0.10 | N/A | 3.42/-0.10 | 3.42/-0.10 | 3.75/-0.10 | N/A | ns |
| | | XC7VX485T | 2.95/-0.26 | N/A | 3.26/-0.26 | 3.26/-0.26 | 3.58/-0.26 | N/A | ns |
| | | XC7VX550T | 3.08/-0.20 | N/A | 3.40/-0.20 | 3.40/-0.20 | 3.74/-0.20 | N/A | ns |
| | | XC7VX690T | 3.08/-0.10 | N/A | 3.40/-0.10 | 3.40/-0.10 | 3.74/-0.10 | N/A | ns |
| | | XC7VX980T | N/A | N/A | 3.39/-0.21 | 3.39/-0.21 | 3.72/-0.21 | N/A | ns |
| | | XC7VX1140T | N/A | 3.00/-0.35 | 3.00/-0.35 | 3.00/-0.35 | 3.27/-0.35 | N/A | ns |
| | | XQ7V585T | N/A | N/A | 3.40/-0.21 | 3.40/-0.21 | 3.72/-0.21 | 3.72/-0.21 | ns |
| | | XQ7VX330T | N/A | N/A | 3.26/-0.26 | 3.26/-0.26 | 3.57/-0.26 | 3.57/-0.26 | ns |
| | | XQ7VX485T | N/A | N/A | 3.26/-0.26 | 3.26/-0.26 | 3.58/-0.26 | 3.58/-0.26 | ns |
| | | XQ7VX690T | N/A | N/A | 3.40/-0.10 | N/A | 3.74/-0.10 | N/A | ns |
| | | XQ7VX980T | N/A | N/A | N/A | 3.39/-0.21 | 3.72/-0.21 | N/A | ns |

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 50: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

| Symbol | Description | Speed Grade | | | | Units |
|--|--|-------------|------------|------------|------------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | |
| T _{PSCS} /T _{PHCS} | Setup/hold of I/O clock for HR I/O banks | -0.36/1.36 | -0.36/1.50 | -0.36/1.70 | -0.36/1.70 | ns |
| | Setup/hold of I/O clock for HP I/O banks | -0.34/1.39 | -0.34/1.53 | -0.34/1.73 | -0.34/1.73 | ns |

Table 51: Sample Window

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------|--|-------------|------------|------|------|-------|
| | | -3 | -2/-2L/-2G | -1 | -1M | |
| T _{SAMP} | Sampling error at receiver pins ⁽¹⁾ | 0.51 | 0.56 | 0.61 | 0.61 | ns |
| T _{SAMP_BUFIO} | Sampling error at receiver pins using BUFIO ⁽²⁾ | 0.30 | 0.35 | 0.40 | 0.40 | ns |

Notes:

- This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-7 T and XT FPGA clock transmitter and receiver data-valid windows.

Table 52: Package Skew

| Symbol | Description | Device | Package | Value | Units |
|----------------------|-----------------------------|------------|---------|-------|-------|
| T _{PKGSKEW} | Package Skew ⁽¹⁾ | XC7V585T | FFG1157 | 232 | ps |
| | | | FFG1761 | 255 | ps |
| | | XC7V2000T | FHG1761 | 308 | ps |
| | | | FLG1925 | 266 | ps |
| | | XC7VX330T | FFG1157 | 170 | ps |
| | | | FFG1761 | 270 | ps |
| | | XC7VX415T | FFG1157 | 203 | ps |
| | | | FFG1158 | 237 | ps |
| | | | FFG1927 | 183 | ps |
| | | XC7VX485T | FFG1157 | 191 | ps |
| | | | FFG1158 | 209 | ps |
| | | | FFG1761 | 274 | ps |
| | | | FFG1927 | 209 | ps |
| | | | FFG1930 | 304 | ps |
| | | XC7VX550T | FFG1158 | 217 | ps |
| | | | FFG1927 | 254 | ps |
| | | XC7VX690T | FFG1157 | 239 | ps |
| | | | FFG1158 | 217 | ps |
| | | | FFG1761 | 284 | ps |
| | | | FFG1926 | 238 | ps |
| | | | FFG1927 | 254 | ps |
| | | | FFG1930 | 287 | ps |
| | | XC7VX980T | FFG1926 | 242 | ps |
| | | | FFG1928 | 199 | ps |
| | | | FFG1930 | 243 | ps |
| | | XC7VX1140T | FLG1926 | 271 | ps |
| | | | FLG1928 | 216 | ps |
| | | | FLG1930 | 279 | ps |
| | | XQ7V585T | RF1157 | 232 | ps |
| | | | RF1761 | 255 | ps |
| XQ7VX330T | RF1157 | 170 | ps | | |
| | RF1761 | 270 | ps | | |
| XQ7VX485T | RF1761 | 274 | ps | | |
| | RF1930 | 304 | ps | | |

Table 52: Package Skew (Cont'd)

| Symbol | Description | Device | Package | Value | Units |
|----------------------|-----------------------------|-----------|---------|-------|-------|
| T _{PKGSKEW} | Package Skew ⁽¹⁾ | XQ7VX690T | RF1157 | 239 | ps |
| | | | RF1158 | 217 | ps |
| | | | RF1761 | 284 | ps |
| | | | RF1930 | 287 | ps |
| | | XQ7VX980T | RF1930 | 287 | ps |

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 53 summarizes the DC specifications of the GTX transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide (UG476)* for further details.

Table 53: GTX Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|--|------------------------------|--------------------------|----------------------|-------|
| DV _{PPOUT} | Differential peak-to-peak output voltage ⁽¹⁾ | Transmitter output swing is set to maximum setting | 1000 | – | – | mV |
| V _{CMOUTDC} | DC common mode output voltage. | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/4$ | | | mV |
| R _{OUT} | Differential output resistance | | – | 100 | – | Ω |
| T _{OSKEW} | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | 12 | ps |
| DV _{PPIN} | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s | 150 | – | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | – | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | – | 2000 | mV |
| V _{IN} | Single-ended input voltage ⁽²⁾ | DC coupled V _{MGTAVTT} = 1.2V | –200 | – | V _{MGTAVTT} | mV |
| V _{CMIN} | Common mode input voltage | DC coupled V _{MGTAVTT} = 1.2V | – | 2/3 V _{MGTAVTT} | – | mV |
| R _{IN} | Differential input resistance | | – | 100 | – | Ω |
| C _{EXT} | Recommended external AC coupling capacitor ⁽³⁾ | | – | 100 | – | nF |

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide (UG476)*, and can result in values lower than reported in this table.
2. Voltage measured at the pin referenced to ground.
3. Other values can be used as appropriate to conform to specific protocols and standards.

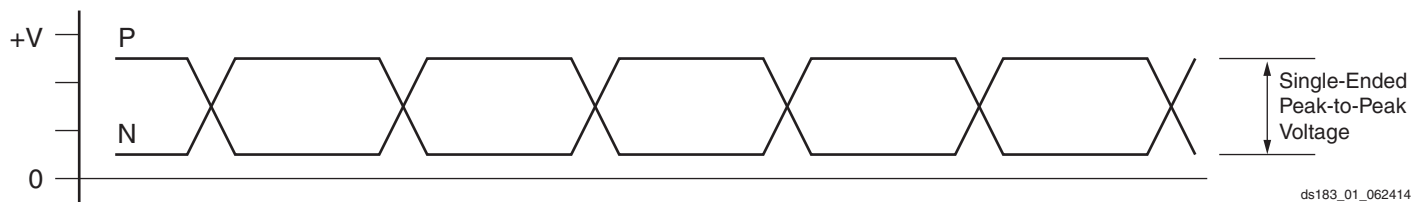


Figure 3: Single-Ended Peak-to-Peak Voltage

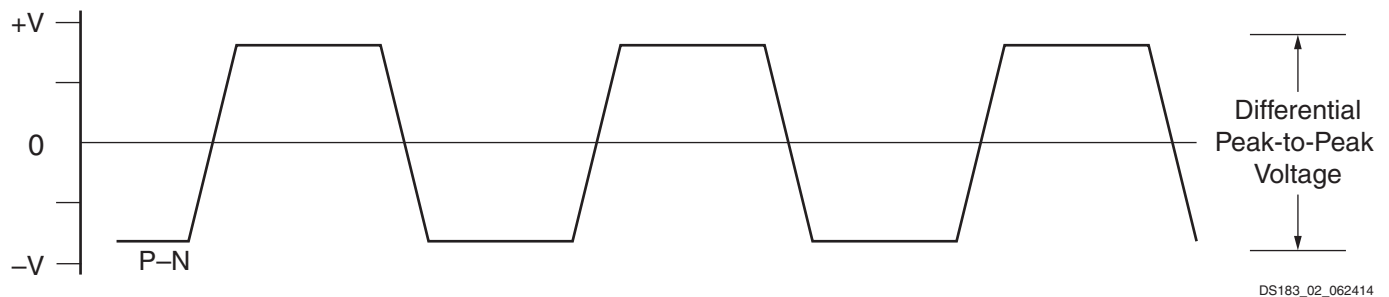


Figure 4: Differential Peak-to-Peak Voltage

Note: In Figure 4, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 54 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide (UG476)* for further details.

Table 54: GTX Transceiver Clock DC Input Level Specification

| Symbol | DC Parameter | Min | Typ | Max | Units |
|--------------------|---|-----|-----|------|-------|
| V _{IDIFF} | Differential peak-to-peak input voltage | 250 | – | 2000 | mV |
| R _{IN} | Differential input resistance | – | 100 | – | Ω |
| C _{EXT} | Required external AC coupling capacitor | – | 100 | – | nF |

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide (UG476)* for further information.

Table 55: GTX Transceiver Performance

| Symbol | Description | Output Divider | Speed Grade | | | Units |
|------------------------------------|--|----------------|----------------|-------------------|-----------------------|-------|
| | | | -3/-2G | -2/-2L | -1/-1M ⁽¹⁾ | |
| F _{GTXMAX} ⁽²⁾ | Maximum GTX transceiver data rate | | 12.5 | 10.3125 | 8.0 | Gb/s |
| F _{GTXMIN} ⁽²⁾ | Minimum GTX transceiver data rate | | 0.500 | 0.500 | 0.500 | Gb/s |
| F _{GTXCRANGE} | CPLL line rate range | 1 | 3.2–6.6 | | | Gb/s |
| | | 2 | 1.6–3.3 | | | Gb/s |
| | | 4 | 0.8–1.65 | | | Gb/s |
| | | 8 | 0.5–0.825 | | | Gb/s |
| | | 16 | N/A | | | Gb/s |
| F _{GTXQRANGE1} | QPLL line rate range 1 | 1 | 5.93–8.0 | 5.93–8.0 | 5.93–8.0 | Gb/s |
| | | 2 | 2.965–4.0 | 2.965–4.0 | 2.965–4.0 | Gb/s |
| | | 4 | 1.4825–2.0 | 1.4825–2.0 | 1.4825–2.0 | Gb/s |
| | | 8 | 0.74125–1.0 | 0.74125–1.0 | 0.74125–1.0 | Gb/s |
| | | 16 | N/A | N/A | N/A | Gb/s |
| F _{GTXQRANGE2} | QPLL line rate range 2 ⁽³⁾ | 1 | 9.8–12.5 | 9.8–10.3125 | N/A | Gb/s |
| | | 2 | 4.9–6.25 | 4.9–5.15625 | N/A | Gb/s |
| | | 4 | 2.45–3.125 | 2.45–2.578125 | N/A | Gb/s |
| | | 8 | 1.225–1.5625 | 1.225–1.2890625 | N/A | Gb/s |
| | | 16 | 0.6125–0.78125 | 0.6125–0.64453125 | N/A | Gb/s |
| F _{GCPLL} RANGE | GTX transceiver CPLL frequency range | | 1.6–3.3 | 1.6–3.3 | 1.6–3.3 | GHz |
| F _{GQPLL} RANGE1 | GTX transceiver QPLL frequency range 1 | | 5.93–8.0 | 5.93–8.0 | 5.93–8.0 | GHz |
| F _{GQPLL} RANGE2 | GTX transceiver QPLL frequency range 2 | | 9.8–12.5 | 9.8–10.3125 | N/A | GHz |

Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.
- Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
- For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 56: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol | Description | Speed Grade | | | Units |
|------------------------|-----------------------------|-------------|--------|--------|-------|
| | | -3/-2G | -2/-2L | -1/-1M | |
| F _{GTXDRPCLK} | GTXDRPCLK maximum frequency | 175.01 | 175.01 | 156.25 | MHz |

Table 57: GTX Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---------------------------------|------------------------|------------------|-----|-----|-------|
| | | | Min | Typ | Max | |
| F _{GCLK} | Reference clock frequency range | -3 speed grade | 60 | – | 700 | MHz |
| | | All other speed grades | 60 | – | 670 | MHz |
| T _{RCLK} | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| T _{FCLK} | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| T _{DCREF} | Reference clock duty cycle | Transceiver PLL only | 40 | 50 | 60 | % |

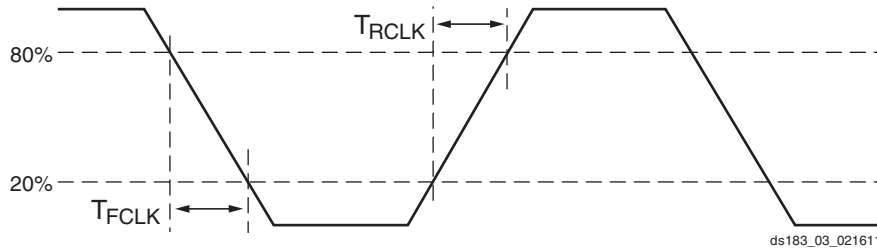


Figure 5: Reference Clock Timing Parameters

Table 58: GTX Transceiver PLL/Lock Time Adaptation

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---|---|------------------|--------|----------------------|-------|
| | | | Min | Typ | Max | |
| T _{LOCK} | Initial PLL lock | | – | – | 1 | ms |
| T _{DLOCK} | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE). | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | 37 x10 ⁶ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. | | – | 50,000 | 2.3 x10 ⁶ | UI |

Table 59: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

| Symbol | Description | Data Width Conditions | | Speed Grade | | | Units |
|--------------------|-----------------------------|-----------------------|--------------------|-----------------------|-----------------------|-----------------------|-------|
| | | Internal Logic | Interconnect Logic | -3/-2G ⁽³⁾ | -2/-2L ⁽³⁾ | -1/-1M ⁽⁴⁾ | |
| F _{TXOUT} | TXOUTCLK maximum frequency | | | 412.500 | 412.500 | 312.500 | MHz |
| F _{RXOUT} | RXOUTCLK maximum frequency | | | 412.500 | 412.500 | 312.500 | MHz |
| F _{TXIN} | TXUSRCLK maximum frequency | 16-bit | 16-bit and 32-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 32-bit | 32-bit | 390.625 | 322.266 | 250.000 | MHz |
| F _{RXIN} | RXUSRCLK maximum frequency | 16-bit | 16-bit and 32-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 32-bit | 32-bit | 390.625 | 322.266 | 250.000 | MHz |
| F _{TXIN2} | TXUSRCLK2 maximum frequency | 16-bit | 16-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 16-bit and 32-bit | 32-bit | 390.625 | 322.266 | 250.000 | MHz |
| | | 32-bit | 64-bit | 195.313 | 161.133 | 125.000 | MHz |
| F _{RXIN2} | RXUSRCLK2 maximum frequency | 16-bit | 16-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 16-bit and 32-bit | 32-bit | 390.625 | 322.266 | 250.000 | MHz |
| | | 32-bit | 64-bit | 195.313 | 161.133 | 125.000 | MHz |

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L, and -2G, a 16-bit datapath can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit datapath can only be used for speeds less than 5.0 Gb/s. For speed grade -1C with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), a 16-bit datapath can only be used for speeds less than 3.8 Gb/s.

Table 60: GTX Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|------------------------------|--|--------------|-------|-----|---------------------|-------|
| F _{GTXTX} | Serial data rate range | | 0.500 | – | F _{GTXMAX} | Gb/s |
| T _{RTX} | TX rise time | 20%–80% | – | 40 | – | ps |
| T _{FTX} | TX fall time | 80%–20% | – | 40 | – | ps |
| T _{LLSKEW} | TX lane-to-lane skew ⁽¹⁾ | | – | – | 500 | ps |
| V _{TXOVBVDP} | Electrical idle amplitude | | – | – | 15 | mV |
| T _{TXOVBTRANSITION} | Electrical idle transition time | | – | – | 140 | ns |
| T _{J12.5} | Total jitter ⁽²⁾⁽⁴⁾ | 12.5 Gb/s | – | – | 0.28 | UI |
| D _{J12.5} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J11.18} | Total jitter ⁽²⁾⁽⁴⁾ | 11.18 Gb/s | – | – | 0.28 | UI |
| D _{J11.18} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J10.3125} | Total jitter ⁽²⁾⁽⁴⁾ | 10.3125 Gb/s | – | – | 0.28 | UI |
| D _{J10.3125} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J9.953} | Total jitter ⁽²⁾⁽⁴⁾ | 9.953 Gb/s | – | – | 0.28 | UI |
| D _{J9.953} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J9.8} | Total jitter ⁽²⁾⁽⁴⁾ | 9.8 Gb/s | – | – | 0.28 | UI |
| D _{J9.8} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J8.0} | Total jitter ⁽²⁾⁽⁴⁾ | 8.0 Gb/s | – | – | 0.30 | UI |
| D _{J8.0} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| T _{J6.6_QPLL} | Total jitter ⁽²⁾⁽⁴⁾ | 6.6 Gb/s | – | – | 0.28 | UI |
| D _{J6.6_QPLL} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |

Table 60: GTX Transceiver Transmitter Switching Characteristics (Cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|------------------------|--|--------------------------|-----|-----|------|-------|
| TJ _{6.6_CPLL} | Total jitter ⁽³⁾⁽⁴⁾ | 6.6 Gb/s | – | – | 0.30 | UI |
| DJ _{6.6_CPLL} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{5.0} | Total jitter ⁽³⁾⁽⁴⁾ | 5.0 Gb/s | – | – | 0.30 | UI |
| DJ _{5.0} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{4.25} | Total jitter ⁽³⁾⁽⁴⁾ | 4.25 Gb/s | – | – | 0.30 | UI |
| DJ _{4.25} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{3.75} | Total jitter ⁽³⁾⁽⁴⁾ | 3.75 Gb/s | – | – | 0.30 | UI |
| DJ _{3.75} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{3.20} | Total jitter ⁽³⁾⁽⁴⁾ | 3.20 Gb/s ⁽⁵⁾ | – | – | 0.20 | UI |
| DJ _{3.20} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.10 | UI |
| TJ _{3.20L} | Total jitter ⁽³⁾⁽⁴⁾ | 3.20 Gb/s ⁽⁶⁾ | – | – | 0.32 | UI |
| DJ _{3.20L} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.16 | UI |
| TJ _{2.5} | Total jitter ⁽³⁾⁽⁴⁾ | 2.5 Gb/s ⁽⁷⁾ | – | – | 0.20 | UI |
| DJ _{2.5} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.08 | UI |
| TJ _{1.25} | Total jitter ⁽³⁾⁽⁴⁾ | 1.25 Gb/s ⁽⁸⁾ | – | – | 0.15 | UI |
| DJ _{1.25} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.06 | UI |
| TJ ₅₀₀ | Total jitter ⁽³⁾⁽⁴⁾ | 500 Mb/s | – | – | 0.10 | UI |
| DJ ₅₀₀ | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.03 | UI |

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 1e⁻¹².
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 61: GTX Transceiver Receiver Switching Characteristics

| Symbol | Description | | Min | Typ | Max | Units |
|--|---|-------------------------------------|-------|-----|---------------------|-------|
| F _{GTXRX} | Serial data rate | | 0.500 | – | F _{GTXMAX} | Gb/s |
| T _{RXELECIDLE} | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| RX _{OOBVDPP} | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| RX _{SST} | Receiver spread-spectrum tracking ⁽¹⁾ | Modulated @ 33 kHz | –5000 | – | 0 | ppm |
| RX _{RL} | Run length (CID) | | – | – | 512 | UI |
| RX _{PPMTOL} | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | –1250 | – | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700 | – | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | –200 | – | 200 | ppm |
| SJ Jitter Tolerance⁽²⁾ | | | | | | |
| JT_SJ _{12.5} | Sinusoidal jitter (QPLL) ⁽³⁾ | 12.5 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{11.18} | Sinusoidal jitter (QPLL) ⁽³⁾ | 11.18 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{10.32} | Sinusoidal jitter (QPLL) ⁽³⁾ | 10.32 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{9.95} | Sinusoidal jitter (QPLL) ⁽³⁾ | 9.95 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{9.8} | Sinusoidal jitter (QPLL) ⁽³⁾ | 9.8 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{8.0} | Sinusoidal jitter (QPLL) ⁽³⁾ | 8.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{6.6_QPLL} | Sinusoidal jitter (QPLL) ⁽³⁾ | 6.6 Gb/s | 0.48 | – | – | UI |
| JT_SJ _{6.6_CPLL} | Sinusoidal jitter (CPLL) ⁽³⁾ | 6.6 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{5.0} | Sinusoidal jitter (CPLL) ⁽³⁾ | 5.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{4.25} | Sinusoidal jitter (CPLL) ⁽³⁾ | 4.25 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{3.75} | Sinusoidal jitter (CPLL) ⁽³⁾ | 3.75 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{3.2} | Sinusoidal jitter (CPLL) ⁽³⁾ | 3.2 Gb/s ⁽⁴⁾ | 0.45 | – | – | UI |
| JT_SJ _{3.2L} | Sinusoidal jitter (CPLL) ⁽³⁾ | 3.2 Gb/s ⁽⁵⁾ | 0.45 | – | – | UI |
| JT_SJ _{2.5} | Sinusoidal jitter (CPLL) ⁽³⁾ | 2.5 Gb/s ⁽⁶⁾ | 0.5 | – | – | UI |
| JT_SJ _{1.25} | Sinusoidal jitter (CPLL) ⁽³⁾ | 1.25 Gb/s ⁽⁷⁾ | 0.5 | – | – | UI |
| JT_SJ ₅₀₀ | Sinusoidal jitter (CPLL) ⁽³⁾ | 500 Mb/s | 0.4 | – | – | UI |
| SJ Jitter Tolerance with Stressed Eye⁽²⁾ | | | | | | |
| JT_TJSE _{3.2} | Total jitter with stressed eye ⁽⁸⁾ | 3.2 Gb/s | 0.70 | – | – | UI |
| JT_TJSE _{6.6} | | 6.6 Gb/s | 0.70 | – | – | UI |
| JT_SJSE _{3.2} | Sinusoidal jitter with stressed eye ⁽⁸⁾ | 3.2 Gb/s | 0.1 | – | – | UI |
| JT_SJSE _{6.6} | | 6.6 Gb/s | 0.1 | – | – | UI |

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 1e⁻¹².
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX in LPM or DFE mode.

GTX Transceiver Protocol Jitter Characteristics

For Table 62 through Table 67, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 62: Gigabit Ethernet Protocol Characteristics (GTX Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|--|------------------|-------|------|-------|
| Gigabit Ethernet Transmitter Jitter Generation | | | | |
| Total transmitter jitter (T_TJ) | 1250 | – | 0.24 | UI |
| Gigabit Ethernet Receiver High Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 1250 | 0.749 | – | UI |

Table 63: XAUI Protocol Characteristics (GTX Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|--|------------------|------|------|-------|
| XAUI Transmitter Jitter Generation | | | | |
| Total transmitter jitter (T_TJ) | 3125 | – | 0.35 | UI |
| XAUI Receiver High Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 3125 | 0.65 | – | UI |

Table 64: PCI Express Protocol Characteristics (GTX Transceivers)⁽¹⁾

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units | |
|---|---|------------------|------|--------|-------|----|
| PCI Express Transmitter Jitter Generation | | | | | | |
| PCI Express Gen 1 | Total transmitter jitter | 2500 | – | 0.25 | UI | |
| PCI Express Gen 2 | Total transmitter jitter | 5000 | – | 0.25 | UI | |
| PCI Express Gen 3 | Total transmitter jitter uncorrelated | 8000 | – | 31.25 | ps | |
| | Deterministic transmitter jitter uncorrelated | | – | 12 | ps | |
| PCI Express Receiver High Frequency Jitter Tolerance | | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance | 2500 | 0.65 | – | UI | |
| PCI Express Gen 2 ⁽²⁾ | Receiver inherent timing error | 5000 | 0.40 | – | UI | |
| | Receiver inherent deterministic timing error | | 0.30 | – | UI | |
| PCI Express Gen 3 | Receiver sinusoidal jitter tolerance | 0.03 MHz–1.0 MHz | 8000 | 1.00 | – | UI |
| | | 1.0 MHz–10 MHz | | Note 3 | – | UI |
| | | 10 MHz–100 MHz | | 0.10 | – | UI |

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 65: CEI-6G and CEI-11G Protocol Characteristics (GTX Transceivers)

| Description | Line Rate (Mb/s) | Interface | Min | Max | Units |
|---|------------------|---------------|-------|-----|-------|
| CEI-6G Transmitter Jitter Generation | | | | | |
| Total transmitter jitter ⁽¹⁾ | 4976–6375 | CEI-6G-SR | – | 0.3 | UI |
| | | CEI-6G-LR | – | 0.3 | UI |
| CEI-6G Receiver High Frequency Jitter Tolerance | | | | | |
| Total receiver jitter tolerance ⁽¹⁾ | 4976–6375 | CEI-6G-SR | 0.6 | – | UI |
| | | CEI-6G-LR | 0.95 | – | UI |
| CEI-11G Transmitter Jitter Generation | | | | | |
| Total transmitter jitter ⁽²⁾ | 9950–11100 | CEI-11G-SR | – | 0.3 | UI |
| | | CEI-11G-LR/MR | – | 0.3 | UI |
| CEI-11G Receiver High Frequency Jitter Tolerance | | | | | |
| Total receiver jitter tolerance ⁽²⁾ | 9950–11100 | CEI-11G-SR | 0.65 | – | UI |
| | | CEI-11G-MR | 0.65 | – | UI |
| | | CEI-11G-LR | 0.825 | – | UI |

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 66: SFP+ Protocol Characteristics (GTX Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|------------------------|-----|------|-------|
| SFP+ Transmitter Jitter Generation | | | | |
| Total transmitter jitter | 9830.40 ⁽¹⁾ | – | 0.28 | UI |
| | 9953.00 | | | |
| | 10312.50 | | | |
| | 10518.75 | | | |
| | 11100.00 | | | |
| SFP+ Receiver Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 9830.40 ⁽¹⁾ | 0.7 | – | UI |
| | 9953.00 | | | |
| | 10312.50 | | | |
| | 10518.75 | | | |
| | 11100.00 | | | |

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 67: CPRI Protocol Characteristics (GTX Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|------------------|------------------------|------------------------|-------|
| CPRI Transmitter Jitter Generation | | | | |
| Total transmitter jitter | 614.4 | – | 0.35 | UI |
| | 1228.8 | – | 0.35 | UI |
| | 2457.6 | – | 0.35 | UI |
| | 3072.0 | – | 0.35 | UI |
| | 4915.2 | – | 0.3 | UI |
| | 6144.0 | – | 0.3 | UI |
| | 9830.4 | – | Note 1 | UI |
| CPRI Receiver Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 614.4 | 0.65 | – | UI |
| | 1228.8 | 0.65 | – | UI |
| | 2457.6 | 0.65 | – | UI |
| | 3072.0 | 0.65 | – | UI |
| | 4915.2 | 0.95 | – | UI |
| | 6144.0 | 0.95 | – | UI |
| | 9830.4 | Note 1 | – | UI |

Notes:

1. Tested per SFP+ specification, see [Table 66](#).

GTH Transceiver Specifications

GTH Transceiver DC Input and Output Levels

Table 68 summarizes the DC specifications of the GTH transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 68: GTH Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|---|------------------------------|--------------------------|----------------------|-------|
| DV _{PPIN} | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s | 150 | – | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | – | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | – | 2000 | mV |
| V _{IN} | Single-ended input voltage ⁽¹⁾ | DC coupled V _{MGTAVTT} = 1.2V | –400 | – | V _{MGTAVTT} | mV |
| V _{CMIN} | Common mode input voltage | DC coupled V _{MGTAVTT} = 1.2V | – | 2/3 V _{MGTAVTT} | – | mV |
| DV _{PPOUT} | Differential peak-to-peak output voltage ⁽²⁾ | Transmitter output swing is set to 1010 | 800 | – | – | mV |
| V _{CMOUTDC} | Common mode output voltage: DC coupled | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/4$ | | | mV |
| V _{CMOUTAC} | Common mode output voltage: AC coupled | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/2$ | | | mV |
| R _{IN} | Differential input resistance | | – | 100 | – | Ω |
| R _{OUT} | Differential output resistance | | – | 100 | – | Ω |
| T _{OSKEW} | Transmitter output pair (TXP and TXN) intra-pair skew | | – | – | 10 | ps |
| C _{EXT} | Recommended external AC coupling capacitor ⁽³⁾ | | – | 100 | – | nF |

Notes:

1. Voltage measured at the pin referenced to ground.
2. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476), and can result in values lower than reported in this table.
3. Other values can be used as appropriate to conform to specific protocols and standards.

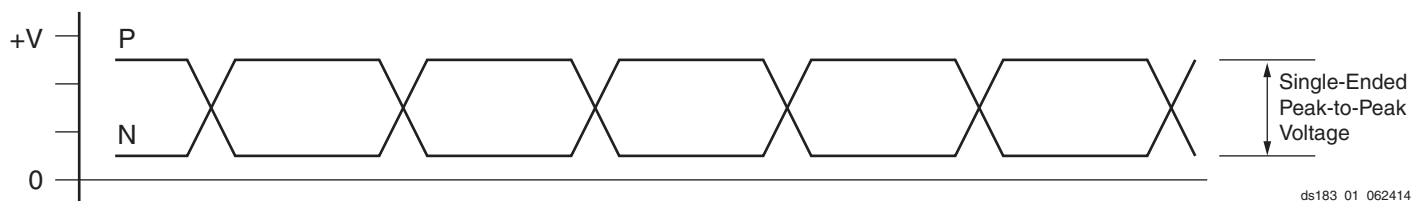
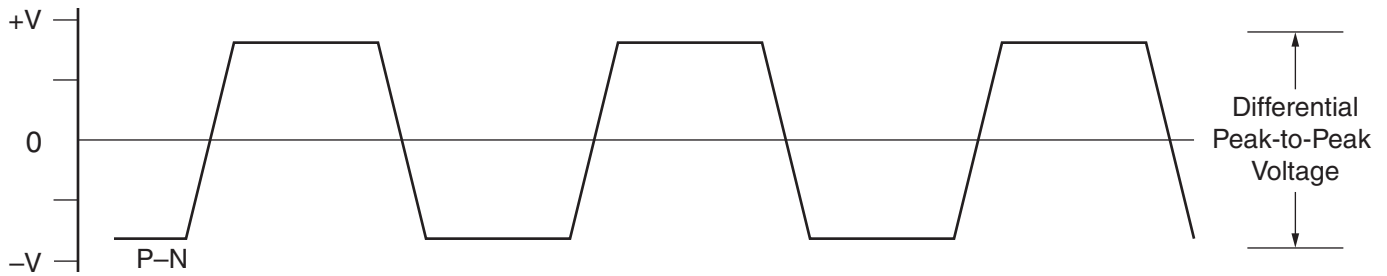


Figure 6: Single-Ended Peak-to-Peak Voltage

ds183_01_062414



DS183_02_062414

Figure 7: Differential Peak-to-Peak Voltage

Note: In Figure 7, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 69 summarizes the DC specifications of the clock input of the GTH transceiver. Consult the 7 Series FPGAs GTX/GTH Transceiver User Guide (UG476) for further details.

Table 69: GTH Transceiver Clock DC Input Level Specification

| Symbol | DC Parameter | Min | Typ | Max | Units |
|--------------------|---|-----|-----|------|-------|
| V _{IDIFF} | Differential peak-to-peak input voltage | 350 | – | 2000 | mV |
| R _{IN} | Differential input resistance | – | 100 | – | Ω |
| C _{EXT} | Required external AC coupling capacitor | – | 100 | – | nF |

GTH Transceiver Switching Characteristics

Consult the 7 Series FPGAs GTX/GTH Transceiver User Guide (UG476) for further information.

Table 70: GTH Transceiver Performance

| Symbol | Description | Output Divider | Speed Grade | | | Units |
|--------------------------|--------------------------------------|----------------|------------------|------------------|--------------------------|-------|
| | | | -3E/-2GE | -2(C/I)/-2LE | -1(C/I/M) ⁽¹⁾ | |
| F _{GTHMAX} | Maximum GTH transceiver data rate | | 13.1 | 11.3 | 8.5 | Gb/s |
| F _{GTHMIN} | Minimum GTH transceiver data rate | | 0.500 | 0.500 | 0.500 | Gb/s |
| F _{GTHCRANGE} | CPLL line rate range | 1 | 3.2–10.3125 | | 3.2–8.0 | Gb/s |
| | | 2 | 1.6–5.16 | | 1.6–4.0 | Gb/s |
| | | 4 | 0.8–2.58 | | 0.8–2.0 | Gb/s |
| | | 8 | 0.5–1.29 | | 0.5–1.0 | Gb/s |
| | | 16 | N/A | | | Gb/s |
| F _{GTHQRANGE1} | QPLL line rate range 1 | 1 | 8.0–11.85 | 8.0–11.3 | 8.0–8.5 | Gb/s |
| | | 2 | 4.0–5.925 | 4.0–5.925 | 4.0–4.25 | Gb/s |
| | | 4 | 2.0–2.9625 | 2.0–2.9625 | 2.0–2.125 | Gb/s |
| | | 8 | 1.0–1.48125 | 1.0–1.48125 | 1.0–1.0625 | Gb/s |
| | | 16 | 0.5–0.740625 | 0.5–0.740625 | 0.5–0.53125 | Gb/s |
| F _{GTHQRANGE2} | QPLL line rate range 2 | 1 | 11.85–13.1 | N/A | | Gb/s |
| | | 2 | 5.925–6.55 | 5.925–6.25 | N/A | Gb/s |
| | | 4 | 2.9625–3.275 | 2.9625–3.125 | N/A | Gb/s |
| | | 8 | 1.48125–1.63 | 1.48125–1.5625 | N/A | Gb/s |
| | | 16 | 0.740625–0.81875 | 0.740625–0.78125 | N/A | Gb/s |
| F _{GCPLL} RANGE | GTH transceiver CPLL frequency range | | 1.6–5.16 | | 1.6–4.0 | GHz |

Table 70: GTH Transceiver Performance (Cont'd)

| Symbol | Description | Output Divider | Speed Grade | | | Units |
|---------------------------|--|----------------|-------------|--------------|--------------------------|-------|
| | | | -3E/-2GE | -2(C/I)/-2LE | -1(C/I/M) ⁽¹⁾ | |
| F _{GQPLL} RANGE1 | GTH transceiver QPLL frequency range 1 | | 8.0–11.85 | 8.0–11.85 | 8.0–8.5 | GHz |
| F _{GQPLL} RANGE2 | GTH transceiver QPLL frequency range 2 | | 11.85–13.1 | 11.85–12.5 | N/A | GHz |

Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note (XAPP555), requires a 4-byte internal data width for operation above 3.8 Gb/s.

Table 71: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|------------------------|-----------------------------|-------------|--------|--------|--------|-------|
| | | -3/-2G | -2L | -2 | -1/-1M | |
| F _{GTHDRPCLK} | GTHDRPCLK maximum frequency | 175.01 | 175.01 | 175.01 | 156.25 | MHz |

Table 72: GTH Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---------------------------------|----------------------|------------------|-----|-----|-------|
| | | | Min | Typ | Max | |
| F _{GCLK} | Reference clock frequency range | | 60 | – | 820 | MHz |
| T _{RCLK} | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| T _{FCLK} | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| T _{DCREF} | Reference clock duty cycle | Transceiver PLL only | 40 | 50 | 60 | % |

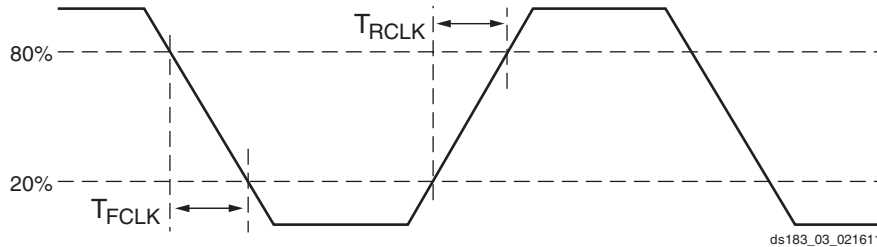


Figure 8: Reference Clock Timing Parameters

Table 73: GTH Transceiver PLL/Lock Time Adaptation

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|--------------------|---|---|------------------|--------|----------------------|-------|
| | | | Min | Typ | Max | |
| T _{LOCK} | Initial PLL lock | | – | – | 1 | ms |
| T _{DLOCK} | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE). | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | 37 x10 ⁶ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. | | – | 50,000 | 2.3 x10 ⁶ | UI |

Table 74: GTH Transceiver User Clock Switching Characteristics⁽¹⁾

| Symbol | Description | Data Width Conditions | | Speed Grade | | | Units |
|--------------------|-----------------------------|-----------------------|--------------------|-------------------------|-----------------------------|--------------------------|-------|
| | | Internal Logic | Interconnect Logic | -3E/-2GE ⁽²⁾ | -2(C/I)/-2LE ⁽²⁾ | -1(C/I/M) ⁽³⁾ | |
| F _{TXOUT} | TXOUTCLK maximum frequency | | | 412.500 | 412.500 | 312.500 | MHz |
| F _{RXOUT} | RXOUTCLK maximum frequency | | | 412.500 | 412.500 | 312.500 | MHz |
| F _{TXIN} | TXUSRCLK maximum frequency | 16-bit | 16-bit and 32-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| F _{RXIN} | RXUSRCLK maximum frequency | 16-bit | 16-bit and 32-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| F _{TXIN2} | TXUSRCLK2 maximum frequency | 16-bit | 16-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 16-bit and 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| | | 32-bit | 64-bit | 204.688 | 176.563 | 132.813 | MHz |
| F _{RXIN2} | RXUSRCLK2 maximum frequency | 16-bit | 16-bit | 412.500 | 412.500 | 312.500 | MHz |
| | | 16-bit and 32-bit | 32-bit | 409.375 | 353.125 | 265.625 | MHz |
| | | 32-bit | 64-bit | 204.688 | 176.563 | 132.813 | MHz |

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit datapath can only be used for line rates less than 6.6 Gb/s.
3. For speed grade -1 with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), a 16-bit datapath can only be used for line rates less than 3.8 Gb/s. For speed grade -1 with V_{CCINT} = 1.0V, a 16-bit datapath can only be used for line rates less than 5.0 Gb/s.

Table 75: GTH Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|------------------------------|--|--------------|-------|-----|----------------------|-------|
| F _{GTHTX} | Serial data rate range | | 0.500 | – | F _{GTHTMAX} | Gb/s |
| T _{RTX} | TX rise time | 20%–80% | – | 40 | – | ps |
| T _{FTX} | TX fall time | 80%–20% | – | 40 | – | ps |
| T _{LLSKEW} | TX lane-to-lane skew ⁽¹⁾ | | – | – | 500 | ps |
| V _{TXOVBVDDP} | Electrical idle amplitude | | – | – | 15 | mV |
| T _{TXOVBTRANSITION} | Electrical idle transition time | | – | – | 140 | ns |
| T _{J13.1} | Total jitter ⁽²⁾⁽⁴⁾ | 13.1 Gb/s | – | – | 0.3 | UI |
| D _{J13.1} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J12.5} | Total jitter ⁽²⁾⁽⁴⁾ | 12.5 Gb/s | – | – | 0.28 | UI |
| D _{J12.5} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J11.3} | Total jitter ⁽²⁾⁽⁴⁾ | 11.3 Gb/s | – | – | 0.28 | UI |
| D _{J11.3} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J10.3125_QPLL} | Total jitter ⁽²⁾⁽⁴⁾ | 10.3125 Gb/s | – | – | 0.28 | UI |
| D _{J10.3125_QPLL} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J10.3125_CPLL} | Total jitter ⁽³⁾⁽⁴⁾ | 10.3125 Gb/s | – | – | 0.33 | UI |
| D _{J10.3125_CPLL} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J9.953} | Total jitter ⁽²⁾⁽⁴⁾ | 9.953 Gb/s | – | – | 0.28 | UI |
| D _{J9.953} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| T _{J9.8} | Total jitter ⁽²⁾⁽⁴⁾ | 9.8 Gb/s | – | – | 0.28 | UI |
| D _{J9.8} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |

Table 75: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

| Symbol | Description | Condition | Min | Typ | Max | Units |
|------------------------|--|--------------------------|-----|-----|------|-------|
| TJ _{8.0_QPLL} | Total jitter ⁽²⁾⁽⁴⁾ | 8.0 Gb/s | – | – | 0.28 | UI |
| DJ _{8.0_QPLL} | Deterministic jitter ⁽²⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| TJ _{8.0_CPLL} | Total jitter ⁽³⁾⁽⁴⁾ | 8.0 Gb/s | – | – | 0.32 | UI |
| DJ _{8.0_CPLL} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.17 | UI |
| TJ _{6.6_CPLL} | Total jitter ⁽³⁾⁽⁴⁾ | 6.6 Gb/s | – | – | 0.30 | UI |
| DJ _{6.6_CPLL} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{5.0} | Total jitter ⁽³⁾⁽⁴⁾ | 5.0 Gb/s | – | – | 0.30 | UI |
| DJ _{5.0} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{4.25} | Total jitter ⁽³⁾⁽⁴⁾ | 4.25 Gb/s | – | – | 0.30 | UI |
| DJ _{4.25} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{3.75} | Total jitter ⁽³⁾⁽⁴⁾ | 3.75 Gb/s | – | – | 0.30 | UI |
| DJ _{3.75} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.15 | UI |
| TJ _{3.20} | Total jitter ⁽³⁾⁽⁴⁾ | 3.20 Gb/s ⁽⁵⁾ | – | – | 0.2 | UI |
| DJ _{3.20} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.1 | UI |
| TJ _{3.20L} | Total jitter ⁽³⁾⁽⁴⁾ | 3.20 Gb/s ⁽⁶⁾ | – | – | 0.32 | UI |
| DJ _{3.20L} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.16 | UI |
| TJ _{2.5} | Total jitter ⁽³⁾⁽⁴⁾ | 2.5 Gb/s ⁽⁷⁾ | – | – | 0.20 | UI |
| DJ _{2.5} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.08 | UI |
| TJ _{1.25} | Total jitter ⁽³⁾⁽⁴⁾ | 1.25 Gb/s ⁽⁸⁾ | – | – | 0.15 | UI |
| DJ _{1.25} | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.06 | UI |
| TJ ₅₀₀ | Total jitter ⁽³⁾⁽⁴⁾ | 500 Mb/s | – | – | 0.1 | UI |
| DJ ₅₀₀ | Deterministic jitter ⁽³⁾⁽⁴⁾ | | – | – | 0.03 | UI |

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTH Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of $1e^{-12}$.
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 76: GTH Transceiver Receiver Switching Characteristics

| Symbol | Description | | Min | Typ | Max | Units |
|--|---|-------------------------------------|-------|-----|---------------------|-------|
| F _{GTHRX} | Serial data rate | | 0.500 | – | F _{GTHMAX} | Gb/s |
| T _{RXELECIDLE} | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| RX _{OOBVDPP} | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| RX _{SST} | Receiver spread-spectrum tracking ⁽¹⁾ | Modulated @ 33 kHz | –5000 | – | 0 | ppm |
| RX _{RL} | Run length (CID) | | – | – | 512 | UI |
| RX _{PPMTOL} | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | –1250 | – | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700 | – | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | –200 | – | 200 | ppm |
| SJ Jitter Tolerance⁽²⁾ | | | | | | |
| JT_SJ _{13.1} | Sinusoidal jitter (QPLL) ⁽³⁾ | 13.1 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{12.5} | Sinusoidal jitter (QPLL) ⁽³⁾ | 12.5 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{11.3} | Sinusoidal jitter (QPLL) ⁽³⁾ | 11.3 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{10.32_QPLL} | Sinusoidal jitter (QPLL) ⁽³⁾ | 10.32 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{10.32_CPLL} | Sinusoidal jitter (CPLL) ⁽³⁾ | 10.32 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{9.8} | Sinusoidal jitter (QPLL) ⁽³⁾ | 9.8 Gb/s | 0.3 | – | – | UI |
| JT_SJ _{8.0_QPLL} | Sinusoidal jitter (QPLL) ⁽³⁾ | 8.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{8.0_CPLL} | Sinusoidal jitter (CPLL) ⁽³⁾ | 8.0 Gb/s | 0.42 | – | – | UI |
| JT_SJ _{6.6_CPLL} | Sinusoidal jitter (CPLL) ⁽³⁾ | 6.6 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{5.0} | Sinusoidal jitter (CPLL) ⁽³⁾ | 5.0 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{4.25} | Sinusoidal jitter (CPLL) ⁽³⁾ | 4.25 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{3.75} | Sinusoidal jitter (CPLL) ⁽³⁾ | 3.75 Gb/s | 0.44 | – | – | UI |
| JT_SJ _{3.2} | Sinusoidal jitter (CPLL) ⁽³⁾ | 3.2 Gb/s ⁽⁴⁾ | 0.45 | – | – | UI |
| JT_SJ _{3.2L} | Sinusoidal jitter (CPLL) ⁽³⁾ | 3.2 Gb/s ⁽⁵⁾ | 0.45 | – | – | UI |
| JT_SJ _{2.5} | Sinusoidal jitter (CPLL) ⁽³⁾ | 2.5 Gb/s ⁽⁶⁾ | 0.5 | – | – | UI |
| JT_SJ _{1.25} | Sinusoidal jitter (CPLL) ⁽³⁾ | 1.25 Gb/s ⁽⁷⁾ | 0.5 | – | – | UI |
| JT_SJ ₅₀₀ | Sinusoidal jitter (CPLL) ⁽³⁾ | 500 Mb/s | 0.4 | – | – | UI |
| SJ Jitter Tolerance with Stressed Eye⁽²⁾ | | | | | | |
| JT_TJSE _{3.2} | Total jitter with stressed eye ⁽⁸⁾ | 3.2 Gb/s | 0.70 | – | – | UI |
| JT_TJSE _{6.6} | | 6.6 Gb/s | 0.70 | – | – | UI |
| JT_SJSE _{3.2} | Sinusoidal jitter with stressed eye ⁽⁸⁾ | 3.2 Gb/s | 0.1 | – | – | UI |
| JT_SJSE _{6.6} | | 6.6 Gb/s | 0.1 | – | – | UI |

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 1e⁻¹².
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX in LPM or DFE mode.

GTH Transceiver Protocol Jitter Characteristics

For Table 77 through Table 82, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 77: Gigabit Ethernet Protocol Characteristics (GTH Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|--|------------------|-------|------|-------|
| Gigabit Ethernet Transmitter Jitter Generation | | | | |
| Total transmitter jitter (T_TJ) | 1250 | – | 0.24 | UI |
| Gigabit Ethernet Receiver High Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 1250 | 0.749 | – | UI |

Table 78: XAUI Protocol Characteristics (GTH Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|--|------------------|------|------|-------|
| XAUI Transmitter Jitter Generation | | | | |
| Total transmitter jitter (T_TJ) | 3125 | – | 0.35 | UI |
| XAUI Receiver High Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 3125 | 0.65 | – | UI |

Table 79: PCI Express Protocol Characteristics (GTH Transceivers)⁽¹⁾

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units | |
|---|---|------------------|------|------------------------|-------|----|
| PCI Express Transmitter Jitter Generation | | | | | | |
| PCI Express Gen 1 | Total transmitter jitter | 2500 | – | 0.25 | UI | |
| PCI Express Gen 2 | Total transmitter jitter | 5000 | – | 0.25 | UI | |
| PCI Express Gen 3 | Total transmitter jitter uncorrelated | 8000 | – | 31.25 | ps | |
| | Deterministic transmitter jitter uncorrelated | | – | 12 | ps | |
| PCI Express Receiver High Frequency Jitter Tolerance | | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance | 2500 | 0.65 | – | UI | |
| PCI Express Gen 2 | Receiver inherent timing error | 5000 | 0.40 | – | UI | |
| | Receiver inherent deterministic timing error | | 0.30 | – | UI | |
| PCI Express Gen 3 | Receiver sinusoidal jitter tolerance | 0.03 MHz–1.0 MHz | 8000 | 1.00 | – | UI |
| | | 1.0 MHz–10 MHz | | Note 3 | – | UI |
| | | 10 MHz–100 MHz | | 0.10 | – | UI |

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 80: CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)

| Description | Line Rate (Mb/s) | Interface | Min | Max | Units |
|---|------------------|---------------|-------|-----|-------|
| CEI-6G Transmitter Jitter Generation | | | | | |
| Total transmitter jitter ⁽¹⁾ | 4976–6375 | CEI-6G-SR | – | 0.3 | UI |
| | | CEI-6G-LR | – | 0.3 | UI |
| CEI-6G Receiver High Frequency Jitter Tolerance | | | | | |
| Total receiver jitter tolerance ⁽¹⁾ | 4976–6375 | CEI-6G-SR | 0.6 | – | UI |
| | | CEI-6G-LR | 0.95 | – | UI |
| CEI-11G Transmitter Jitter Generation | | | | | |
| Total transmitter jitter ⁽²⁾ | 9950–11100 | CEI-11G-SR | – | 0.3 | UI |
| | | CEI-11G-LR/MR | – | 0.3 | UI |
| CEI-11G Receiver High Frequency Jitter Tolerance | | | | | |
| Total receiver jitter tolerance ⁽²⁾ | 9950–11100 | CEI-11G-SR | 0.65 | – | UI |
| | | CEI-11G-MR | 0.65 | – | UI |
| | | CEI-11G-LR | 0.825 | – | UI |

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 81: SFP+ Protocol Characteristics (GTH Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|------------------------|-----|------|-------|
| SFP+ Transmitter Jitter Generation | | | | |
| Total transmitter jitter | 9830.40 ⁽¹⁾ | – | 0.28 | UI |
| | 9953.00 | | | |
| | 10312.50 | | | |
| | 10518.75 | | | |
| | 11100.00 | | | |
| SFP+ Receiver Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 9830.40 ⁽¹⁾ | 0.7 | – | UI |
| | 9953.00 | | | |
| | 10312.50 | | | |
| | 10518.75 | | | |
| | 11100.00 | | | |

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 82: CPRI Protocol Characteristics (GTH Transceivers)

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|------------------|--------|--------|-------|
| CPRI Transmitter Jitter Generation | | | | |
| Total transmitter jitter | 614.4 | – | 0.35 | UI |
| | 1228.8 | – | 0.35 | UI |
| | 2457.6 | – | 0.35 | UI |
| | 3072.0 | – | 0.35 | UI |
| | 4915.2 | – | 0.3 | UI |
| | 6144.0 | – | 0.3 | UI |
| | 9830.4 | – | Note 1 | UI |
| CPRI Receiver Frequency Jitter Tolerance | | | | |
| Total receiver jitter tolerance | 614.4 | 0.65 | – | UI |
| | 1228.8 | 0.65 | – | UI |
| | 2457.6 | 0.65 | – | UI |
| | 3072.0 | 0.65 | – | UI |
| | 4915.2 | 0.95 | – | UI |
| | 6144.0 | 0.95 | – | UI |
| | 9830.4 | Note 1 | – | UI |

Notes:

1. Tested per SFP+ specification, see [Table 81](#).

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 83: Maximum Performance for PCI Express Designs

| Symbol | Description | Speed Grade | | | Units |
|-----------------------|--------------------------------|-----------------------|-----------------------|--------|-------|
| | | -3 | -2/-2L/-2G | -1/1M | |
| F _{PIPECLK} | Pipe clock maximum frequency | 250.00 | 250.00 | 250.00 | MHz |
| F _{USERCLK} | User clock maximum frequency | 500.00 ⁽¹⁾ | 500.00 ⁽¹⁾ | 250.00 | MHz |
| F _{USERCLK2} | User clock 2 maximum frequency | 250.00 | 250.00 | 250.00 | MHz |
| F _{DRPCLK} | DRP clock maximum frequency | 250.00 | 250.00 | 250.00 | MHz |

Notes:

1. PCI Express x8 Gen 2 operation is only supported in -2 and -3 speed grades for devices that have GTX transceivers. Refer to *7 Series FPGAs Integrated Block for PCI Express Product Guide (PG054)* for specific supported core configurations.
2. PCI Express Gen 3 operation is only supported in -2 and -3 speed grades for devices that have GTH transceivers. Refer to *Virtex-7 FPGA Gen3 Integrated Block for PCI Express v3.0 (PG023)* for specific supported core configurations.

XADC Specifications

Table 84: XADC Specifications

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|------------|--|------|-----|-------------|---------------------|
| $V_{CCADC} = 1.8V \pm 5\%$, $V_{REFP} = 1.25V$, $V_{REFN} = 0V$, $ADCCLK = 26\text{ MHz}$, $T_j = -40^\circ\text{C}$ to 100°C , Typical values at $T_j = +40^\circ\text{C}$ | | | | | | |
| ADC Accuracy⁽¹⁾ | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity ⁽²⁾ | INL | | – | – | ± 3 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ± 1 | LSBs |
| Offset Error | | Offset calibration enabled | – | – | ± 6 | LSBs |
| Gain Error | | Gain calibration disabled | – | – | ± 0.5 | % |
| Offset Matching | | Offset calibration enabled | – | – | 4 | LSBs |
| Gain Matching | | Gain calibration disabled | – | – | 0.3 | % |
| Sample Rate | | | – | – | 1 | MS/s |
| Signal to Noise Ratio ⁽²⁾ | SNR | $F_{SAMPLE} = 500\text{KS/s}$, $F_{IN} = 20\text{ kHz}$ | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion ⁽²⁾ | THD | $F_{SAMPLE} = 500\text{KS/s}$, $F_{IN} = 20\text{ kHz}$ | – | 70 | – | dB |
| ADC Accuracy at Extended Temperatures | | | | | | |
| Resolution | | $T_j = -55^\circ\text{C}$ to 125°C | 10 | – | – | Bits |
| Integral Nonlinearity ⁽²⁾ | INL | $T_j = -55^\circ\text{C}$ to 125°C | – | – | ± 1 | LSB (at 10 bits) |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic, $T_j = -55^\circ\text{C}$ to 125°C | – | – | ± 1 | |
| Analog Inputs⁽³⁾ | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | V_{CCADC} | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | kHz |
| On-Chip Sensors | | | | | | |
| Temperature Sensor Error | | $T_j = -40^\circ\text{C}$ to 100°C . | – | – | ± 4 | $^\circ\text{C}$ |
| | | $T_j = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | – | – | ± 6 | $^\circ\text{C}$ |
| Supply Sensor Error | | Measurement range of V_{CCAUX} $1.8V \pm 5\%$ $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$ | – | – | ± 1 | % |
| | | Measurement range of V_{CCAUX} $1.8V \pm 5\%$ $T_j = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | – | – | ± 2 | % |
| Conversion Rate⁽⁴⁾ | | | | | | |
| Conversion Time - Continuous | t_{CONV} | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | t_{CONV} | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |

Table 84: XADC Specifications (Cont'd)

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|-------------------------------------|-------------------|---|--------|------|--------|-------|
| DCLK Duty Cycle | | | 40 | – | 60 | % |
| XADC Reference⁽⁵⁾ | | | | | | |
| External Reference | V _{REFP} | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| On-Chip Reference | | Ground V _{REFP} pin to AGND, T _j = –40°C to 100°C | 1.2375 | 1.25 | 1.2625 | V |

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for the bitstream option XADCEnhancedLinearity = ON.
- For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter (UG480)*.
- For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter (UG480)*.
- Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 85: Configuration Switching Characteristics

| Symbol | Description | Virtex-7 T and XT Devices | Speed Grade | | | Units |
|--|--|---------------------------|-------------|------------|--------|-------------|
| | | | -3 | -2/-2L/-2G | -1/-1M | |
| Power-up Timing Characteristics | | | | | | |
| T _{PL} ⁽¹⁾ | Program latency | | 5 | 5 | 5 | ms, Max |
| T _{POR} ⁽¹⁾ | Power-on reset (50ms ramp rate time) | | 10/50 | 10/50 | 10/50 | ms, Min/Max |
| | Power-on reset (1ms ramp rate time) | | 10/35 | 10/35 | 10/35 | ms, Min/Max |
| T _{PROGRAM} | Program pulse width | | 250 | 250 | 250 | ns, Min |
| CCLK Output (Master Mode) | | | | | | |
| T _{ICCK} | Master CCLK output delay | | 150 | 150 | 150 | ns, Min |
| T _{MCKL} | Master CCLK clock Low time duty cycle | | 40/60 | 40/60 | 40/60 | %, Min/Max |
| T _{MCKH} | Master CCLK clock High time duty cycle | | 40/60 | 40/60 | 40/60 | %, Min/Max |
| F _{MCK} | Master CCLK frequency | | 100 | 100 | 100 | MHz, Max |
| | Master CCLK frequency for AES encrypted x16 | | 50 | 50 | 50 | MHz, Max |
| F _{MCK_START} | Master CCLK frequency at start of configuration | | 3 | 3 | 3 | MHz, Typ |
| F _{MCKTOL} | Frequency tolerance, master mode with respect to nominal CCLK. | | ±50 | ±50 | ±50 | %, Max |
| CCLK Input (Slave Modes) | | | | | | |
| T _{SCCKL} | Slave CCLK clock minimum Low time | | 2.5 | 2.5 | 2.5 | ns, Min |
| T _{SCCKH} | Slave CCLK clock minimum High time | | 2.5 | 2.5 | 2.5 | ns, Min |
| F _{SCCK} | Slave CCLK frequency | | 100 | 100 | 100 | MHz, Max |
| EMCCLK Input (Master Mode) | | | | | | |
| T _{EMCKL} | External master CCLK Low time | | 2.5 | 2.5 | 2.5 | ns, Min |
| T _{EMCKH} | External master CCLK High time | | 2.5 | 2.5 | 2.5 | ns, Min |
| F _{EMCK} | External master CCLK frequency | | 100 | 100 | 100 | MHz, Max |

Table 85: Configuration Switching Characteristics (Cont'd)

| Symbol | Description | Virtex-7 T and XT Devices | Speed Grade | | | Units |
|---|--|---|-------------|------------|-----------|-------------|
| | | | -3 | -2/-2L/-2G | -1/-1M | |
| Internal Configuration Access Port | | | | | | |
| F _{ICAPCK} | Internal configuration access port (ICAPE2) | Master SLR ICAP accessing the entire device | 70.00 | 70.00 | 70.00 | MHz, Max |
| | | SLR ICAP accessing the local SLR | 100.00 | 100.00 | 100.00 | MHz, Max |
| | | All other devices | 100.00 | 100.00 | 100.00 | MHz, Max |
| Master/Slave Serial Mode Programming Switching | | | | | | |
| T _{DCCK} /T _{CCKD} | DIN setup/hold | | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | ns, Min |
| T _{CCO} | DOUT clock to out | | 8.0 | 8.0 | 8.0 | ns, Max |
| SelectMAP Mode Programming Switching | | | | | | |
| T _{SMDCCK} /T _{SMCCKD} | D[31:00] setup/hold | | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | ns, Min |
| T _{SMCSCCK} /T _{SMCCKCS} | CSI_B setup/hold | | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | ns, Min |
| T _{SMWCCK} /T _{SMCCKW} | RDWR_B setup/hold | | 10.0/0.0 | 10.0/0.0 | 10.0/0.0 | ns, Min |
| T _{SMCKCSO} | CSO_B clock to out (330 Ω pull-up resistor required) | | 7.0 | 7.0 | 7.0 | ns, Max |
| T _{SMCO} | D[31:00] clock to out in readback | | 8.0 | 8.0 | 8.0 | ns, Max |
| F _{RBCK} | Readback frequency | SLR-based | N/A | 70 | 70 | MHz, Max |
| | | All other devices | 100 | 100 | 100 | MHz, Max |
| Boundary-Scan Port Timing Specifications | | | | | | |
| T _{TAPTCK} /T _{TCKTAP} | TMS and TDI setup/hold | SLR-based | N/A | 9.0/2.0 | 9.0/2.0 | ns, Min |
| | | All other devices | 3.0/2.0 | 3.0/2.0 | 3.0/2.0 | ns, Min |
| T _{TCKTDO} | TCK falling edge to TDO output | SLR-based | N/A | 17 | 17 | ns, Max |
| | | All other devices | 7.0 | 7.0 | 7.0 | ns, Max |
| F _{TCK} | TCK frequency | SLR-based | N/A | 20 | 20 | MHz, Max |
| | | All other devices | 66 | 66 | 66 | MHz, Max |
| BPI Flash Master Mode Programming Switching | | | | | | |
| T _{BPICCO} ⁽²⁾ | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out | | 8.5 | 8.5 | 8.5 | ns, Max |
| T _{BPIDCC} /T _{BPICCD} | D[15:00] setup/hold | | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | ns, Min |
| SPI Flash Master Mode Programming Switching | | | | | | |
| T _{SPIDCC} /T _{SPICCD} | D[03:00] setup/hold | | 3.0/0.0 | 3.0/0.0 | 3.0/0.0 | ns, Min |
| T _{SPICCM} | MOSI clock to out | | 8.0 | 8.0 | 8.0 | ns, Max |
| T _{SPICFC} | FCS_B clock to out | | 8.0 | 8.0 | 8.0 | ns, Max |
| STARTUPE2 Ports | | | | | | |
| T _{USRCLKO} | STARTUPE2 USRCLKO input to CCLK output | | 0.50/6.00 | 0.50/6.70 | 0.50/7.50 | ns, Min/Max |
| F _{CFGMCLK} | STARTUPE2 CFGMCLK output frequency | | 65.00 | 65.00 | 65.00 | MHz, Typ |
| F _{CFGMCLKTOL} | STARTUPE2 CFGMCLK output frequency tolerance | | ±50 | ±50 | ±50 | %, Max |
| Device DNA Access Port | | | | | | |
| F _{DNACK} | DNA access port (DNA_PORT) | | 100.00 | 100.00 | 100.00 | MHz, Max |

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* ([UG470](#)).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 86 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide (UG470)*.

Table 86: eFUSE Programming Conditions⁽¹⁾

| Symbol | Description | Min | Typ | Max | Units |
|----------|----------------------------|-----|-----|-----|-------|
| I_{FS} | V_{CCAUX} supply current | – | – | 115 | mA |
| t_j | Temperature range | 15 | – | 125 | °C |

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document.

| Date | Version | Description |
|------------|---------|---|
| 03/01/2011 | 1.0 | Initial Xilinx release. |
| 10/05/2011 | 1.1 | Removed the XC7V285T, XC7V450T, and XC7V855T devices from the entire data sheet. Added the XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T devices to the entire data sheet. Replaced -1L with -2L throughout this data sheet. Added the extended temperature range discussion to page 1 . Updated Min/Max values and removed Note 5 from Table 2 . Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8 . Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7 . Updated V_{ICM} in Table 12 and Table 13 . Added Note 1 to Table 12 . Updated Table 86 including adding Note 1 . Added Table 13 . Revised the reference clock maximum frequency (F_{GCLK}) in Table 57 . Added Table 59 . Added GTH Transceiver Specifications section. Removed erroneous instances of HSTL_III from Table 20 . Removed the <i>I/O Standard Adjustment Measurement Methodology</i> section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT_JIT}$ in Table 28 . Added T_{AS}/T_{AH} to Table 30 . Added $T_{RDCK_DI_WF_NC}/T_{RDCK_DI_WF_NC}$ and $T_{RDCK_DI_RF}/T_{RDCK_DI_RF}$ to Table 33 . Completely updated the specifications in Table 85 . Updated $MMCM_F_{INDUTY}$ and added $F_{INJITTER}$, $T_{OUTJITTER}$, and $T_{EXTFDVAR}$ and Note 3 to Table 40 . Updated the AC Switching Characteristics section. Updated the Table 52 package list. Updated the Notice of Disclaimer . |
| 11/07/2011 | 1.2 | Added -2G speed grade, where appropriate, throughout document. Revised the V_{OCM} specification in Table 12 . Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20 . Added MMCM to the symbol names of a few specifications in Table 40 and PLL to the symbol names in Table 41 . In Table 42 through Table 49 , updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 51 . |
| 02/13/2012 | 1.3 | Updated summary description on page 1 . In Table 2 , revised V_{CCO} for the 3.3V HR I/O banks and updated T_j . Added typical numbers to Table 3 . Updated the notes in Table 6 . Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8 . Rearranged Table 9 , added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11 . Revised the specifications in Table 12 and Table 13 . Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 84 . Revised DDR LVDS transmitter data width in Table 17 . Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 30 as they are no longer applicable. Updated specifications in Table 85 . Updated Note 1 in Table 39 . In the GTX Transceiver Specifications section: Revised V_{IN} , and added I_{DCIN} and I_{DCOUT} to Table 53 . Updated and added notes to Table 55 . In Table 57 , revised F_{GCLK} , removed T_{PHASE} , and added T_{DLOCK} . Revised specifications and added Note 2 to Table 59 . Added Table 60 and Table 61 along with GTX Transceiver Protocol Jitter Characteristics in Table 62 through Table 67 . |

| Date | Version | Description |
|------------|---------|---|
| 05/23/2012 | 1.4 | <p>Reorganized entire data sheet including adding Table 46 and Table 50.</p> <p>Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing section with regards to GTX/GTH transceivers. Updated many parameters in Table 9, including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 17 and removed notes 2 and 3. Updated Table 18.</p> <p>Updated the AC Switching Characteristics section based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and v1.05 for the -2L (0.9V) speed specifications throughout the document.</p> <p>In Table 33, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 57. Updated many of the XADC specifications in Table 84 and added Note 2. Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 85 to Table 40 and Table 41.</p> |
| 08/03/2012 | 1.5 | <p>Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 13 and Note 14. Updated parameters in Table 3. Added Table 4 and Table 5. Updated the values for in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11.</p> <p>Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.2 speed specifications throughout the document with appropriate changes to Table 15 and Table 16 including production release of the XC7VX485T in the -2 and -1 speed designations.</p> <p>Added notes and specifications to Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$.</p> <p>Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 30.</p> <p>Rearranged Table 53 including moving some parameters to Table 1. Added Table 58. Updated Table 59. In Table 61, updated SJ Jitter Tolerance with Stressed Eye section, page 57 and Note 8. Added Note 1, Note 2, and Note 2 to Table 64. Added Note 1 and Note 2 to Table 65, and line rate ranges. Updated Table 66 including adding Note 1. Updated Table 67 including adding Note 1.</p> <p>In Table 84 updated Note 1 and added Note 4. In Table 85, updated T_{POR} and F_{EMCK}.</p> |
| 09/20/2012 | 1.6 | <p>Removed the XC7V1500T device from data sheet. In Table 2, revised V_{CCINT} and V_{CCBRAM} and added Note 3. Updated some of the values in Table 7. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -2 and -1 speed designations. Added values for the XC7V585T in Table 52. Updated Note 2 in Table 60.</p> |
| 09/26/2012 | 1.7 | <p>Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -3 speed designation.</p> |
| 10/19/2012 | 1.8 | <p>Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -2L (1.0V) speed designation.</p> <p>Removed -2L (0.9V) speed specifications from data sheet, this change includes edits to V_{CCINT} and V_{CCBRAM} in Table 2, editing Note 1 and removing Note 2 in Table 55. Also in Table 55, updated the F_{GTXMAX}, $F_{GTXQRANGE1}$, and $F_{GOPLLRange1}$ specification for -1 speed grade from 6.6 Gb/s to 8.0 Gb/s. Edited Note 4 in Table 59 and Note 3 in Table 74.</p> |
| 12/12/2012 | 1.9 | <p>Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.3 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -3 and -2L(1.0V) speed designations. Updated the notes in Table 52.</p> <p>Updated GTH Transceiver Specifications including removal of GTH Transceiver DC Characteristics section (use the XPE (download at http://www.xilinx.com/power)). Updated Table 70 and added Table 73, Table 75, and Table 76. Removed Note 4 from Table 84.</p> |
| 12/24/2012 | 1.10 | <p>Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.4 and Vivado 2012.4 speed specifications throughout the document. Revised the XC7V2000T in the -1 and -2 speed designations Table 15 to preliminary.</p> <p>Added the GTH Transceiver Protocol Jitter Characteristics section. Updated T_{TCKTDO} and added Internal Configuration Access Port section to Table 85.</p> |
| 01/31/2013 | 1.11 | <p>Added Note 2 to Table 2. Revised Table 15 and Table 16 to include production release of the XC7V2000T in the -1 and -2 speed specifications. Updated Note 1 in Table 37. Updated the notes in Table 39, Table 42 through Table 45, Table 48, and Table 49. In Table 68, updated D_{VPPIN}. In Table 69, updated V_{IDIFF}. Removed T_{LOCK} and T_{PHASE} from Table 72. Updated T_{DLOCK} in Table 73.</p> |

| Date | Version | Description |
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| 03/07/2013 | 1.12 | Updated the AC Switching Characteristics section, based upon Table 14 , for the ISE 14.5 and Vivado 2013.1 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7VX690T. Revised D_{VPP_OUTPUT} in Table 68 . Updated values in Table 69 and Table 76 . Removed Note 1 from Table 70 . Updated $MMCM_F_{PFDMAX}$ in Table 40 and PLL_F_{PFDMAX} in Table 41 . Added skew values to Table 52 . |
| 03/27/2013 | 1.13 | In Table 7 , added values for the XC7VX330T and XC7VX415T devices. Revised Table 15 and Table 16 to include production release of the XC7VX330T and XC7VX415T. In Table 18 , updated the table title, LPDDR2 values, and removed Note 3. Removed Note 2: <i>For QPLL line rate, the maximum line rate with the divider N set to 66 is 10.3125 Gb/s</i> from Table 70 . |
| 04/17/2013 | 1.14 | Updated the AC Switching Characteristics section with production release changes to Table 15 and Table 16 for XC7VX550T for all speed specifications. In Table 1 , revised V_{IN} (I/O input voltage) to match values in Table 4 and Table 5 , and combined Note 4 with old Note 5 and then added new Note 5 . Revised V_{IN} description and added Note 9 in Table 2 . Updated first 3 rows in Table 4 and Table 5 . Updated values and added new values to Table 7 . Also revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 , Table 4 , and Table 5 . Added Note 1 to Table 12 and Table 13 . Throughout the data sheet (Table 31 , Table 32 , and Table 47) removed the obvious note "A Zero "0" Hold Time listing indicates no hold time or a negative hold time." Updated and clarified USRCLK data in Table 59 and Table 74 . |
| 05/07/2013 | 1.15 | Revised Table 15 and Table 16 for the production release of the XC7V2000T and XC7VX980T devices. |
| 05/15/2013 | 1.16 | Revised Table 15 and Table 16 for the production release of the XC7VX1140T devices. |
| 09/04/2013 | 1.17 | In Table 1 , updated I_{DCIN} and I_{DCOUT} section for cases when floating, at $V_{MGTAVTT}$, or GND. Removed notes from Table 7 . Updated $F_{MAX_PREADD_MULT_NOADREG_PATDET}$ for -1 speed grade in Table 34 . In Table 59 and Table 74 , updated number of bits in Internal Logic column for F_{TXIN2} and F_{RXIN2} from 64 to 32. Updated Note 8 and description of F_{GTXRX} in Table 61 . Updated $F_{GTHQRANGE1}$, $F_{GTHQRANGE2}$, $F_{GQPLLRANGE1}$, and $F_{GQPLLRANGE2}$ in Table 70 . Updated clock names and Note 2 and Note 3 in Table 74 . Removed $T_{J_{6.6_QPLL}}$ and $D_{J_{6.6_QPLL}}$ from Table 75 . Updated description of F_{GTHRX} , removed $JT_SJ_{6.6_QPLL}$, and updated Note 8 in Table 76 . Replaced BitGen with bitstream in Note 2 of Table 84 . Updated F_{RBCK} , T_{TAPTCK}/T_{TCKTAP} , T_{CKTDO} , and F_{TCK} in Table 85 . |
| 11/26/2013 | 1.18 | Added Virtex-7Q defense-grade devices throughout. Added -1M speed grade throughout. Added reference to 7 Series FPGAs Overview and Defense-Grade 7 Series FPGAs Overview in Introduction . In Table 2 , added junction temperature operating range for military (M) devices and updated Note 6 . In Table 3 , removed commercial (C), industrial (I), and extended (E) from descriptions of R_{IN_TERM} . Updated temperature ranges in Table 4 and Table 5 . Added $T_J = 125^{\circ}C$ to Conditions column for $T_{VCCO2VCCAUX}$ in Table 8 . Updated to ISE Design Suite 14.7 and Vivado Design Suite 2013.3 in AC Switching Characteristics . Added 1.05 and 1.06 rows to Table 14 . Added -1M speed grade to Table 70 and Table 74 . Added $T_{USRCLKO}$ and F_{DNACK} to Table 85 . |
| 03/04/2014 | 1.19 | In Table 2 , removed 1.0V from Note 6 and added Note 7 . Added Note 2 to Table 4 . Added Note 2 and updated Note 3 in Table 5 . Updated to Vivado Design Suite 2013.4 in AC Switching Characteristics . Revised Table 15 and Table 16 for the production release of the XQ7VX690T devices. Added HSUL_12_F, DIFF_HSUL_12_F, MOBILE_DDR_S, MOBILE_DDR_F, DIFF_MOBILE_DDR_S, and DIFF_MOBILE_DDR_F standards to and updated values in Table 19 . Added HSUL_12_F, DIFF_HSUL_12_F, DIFF_HSUL_12_DCI_S, and DIFF_HSUL_12_DCI_F standards to and updated values in Table 20 . Removed notes from Table 19 and Table 20 . Removed introductory paragraph of Device Pin-to-Pin Output Parameter Guidelines and Device Pin-to-Pin Input Parameter Guidelines . Enhanced precision of $F_{GTHDRPCLK}$ numbers in Table 71 . Added Note 1 to Table 83 . Updated display format of "ADC Accuracy at Extended Temperatures" section in Table 84 . Updated F_{ICAPCK} in Table 85 . |
| 04/11/2014 | 1.20 | Revised Table 15 and Table 16 for the production release of the XQ7VX485T devices. Updated Note 1 in Table 83 . |
| 07/01/2014 | 1.21 | In Table 4 and Table 5 , updated Note 2 per the customer notice XCN14014: 7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update . In Power-On/Off Power Supply Sequencing , added sentence about there being no recommended sequence for supplies not shown. In Table 15 , moved all XQ7V585T, XQ7VX330T, and XQ7VX980T speed grades from Preliminary to Production. In Table 16 , added production software for -2, -2L, -1, and -1M speed grades of XQ7V585T and XQ7VX330T, and -2L and -1M speed grades of XQ7VX980T. Added Note 3 to Table 18 . In Table 28 , added attribute REFCLK frequency of 400 MHz to $F_{IDELAYCTRL_REF}$ and average tap delay at 400 MHz to Note 1 . Updated description of T_{ICKOFF} in Table 42 and added Note 2 . Updated description of $T_{ICKOFFAR}$ in Table 43 and added Note 2 . In Table 52 , updated $T_{PKGSKEW}$ for XQ7VX980T to 287 ps. In Table 53 , moved DV_{PPOUT} value of 1000 mV from Max to Min column, updated V_{IN} DC parameter description, and added Note 2 . |

| Date | Version | Description |
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| 07/01/2014 | 1.21 (Cont'd) | Added "peak-to-peak" to labels in Figure 3 and Figure 4 . Added note after Figure 4 . In Table 68 , updated V_{IN} DC parameter description, moved DV_{PPOUT} value of 800 mV from Max to Min column, and added Note 1 . Added "peak-to-peak" to labels in Figure 6 and Figure 7 . Added note after Figure 7 . In Table 83 , updated Note 1 and added Note 2 . In Table 85 , replaced USRCCLK Output with STARTUPE2 Ports and added F_{CFGCLK} and $F_{CFGCLKTOL}$. |
| 03/06/2015 | 1.22 | Updated Note 3 in Table 6 . In Table 12 , changed maximum V_{ICM} value from 1.425V to 1.500V. Removed minimum sample rate specification from Table 84 . |
| 06/23/2015 | 1.23 | Added FFV1157, FFV1158, FFV1761, FFV1927, and RF1158 packages to Table 52 . |
| 09/24/2015 | 1.24 | Added introductory paragraph before Table 18 . Updated Note 3 in Table 18 . Removed note about PCI-SIG 3.0 certification and compliance test boards from Table 64 and Table 79 . Updated F_{ICAPCK} description from ICAPE3 to ICAPE2 in Table 85 . |
| 02/02/2016 | 1.25 | Added I/O Standard Adjustment Measurement Methodology . |
| 03/28/2016 | 1.26 | Updated V_{MEAS} for LVC MOS33, LVTTTL, and PCI33_3 in Table 22 . |
| 04/06/2017 | 1.27 | In Table 28 , changed $T_{IDELAYRESOLUTION}$ units from ps to μ s. Removed FFV1157, FFV1158, FFV1761, and FFV1927 packages from Table 52 per the customer notice XCEN16022: Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages . |
| 03/13/2019 | 1.28 | Updated Note 3 in Table 3 . |

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